Area Selective Deposition Workshop 2017
April 21st, Eindhoven, The Netherlands

TOKYO ELECTRON

Advanced process technologies for sub-10nm patterning

April 21, 2017

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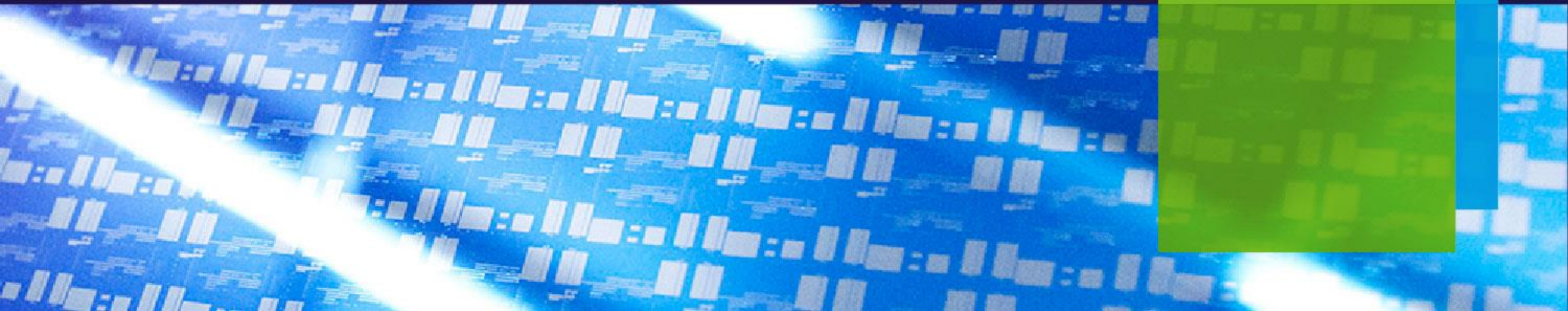
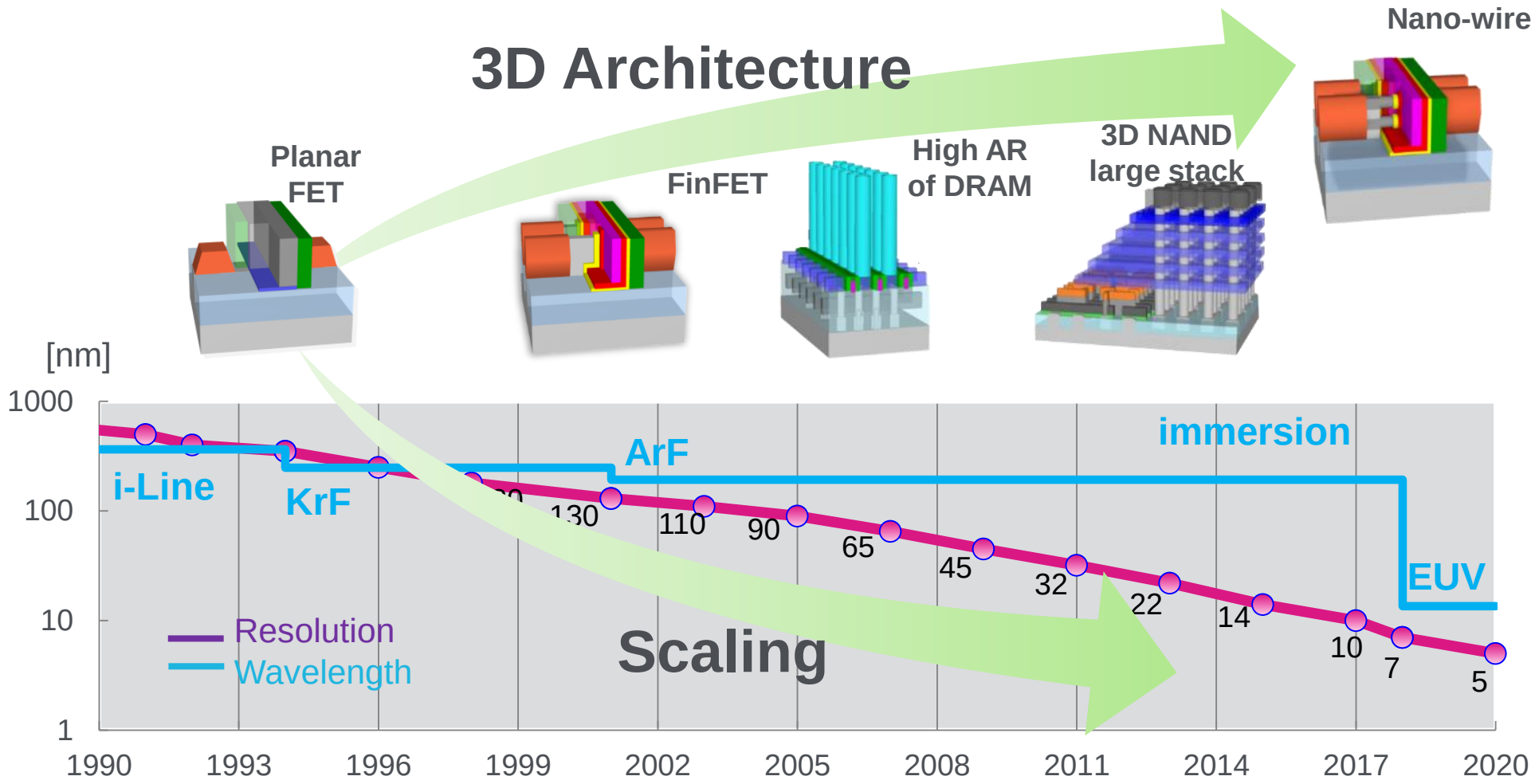


Contents

- Technology trends
- Patterning challenges and approach
- Process technology examples
- Summary

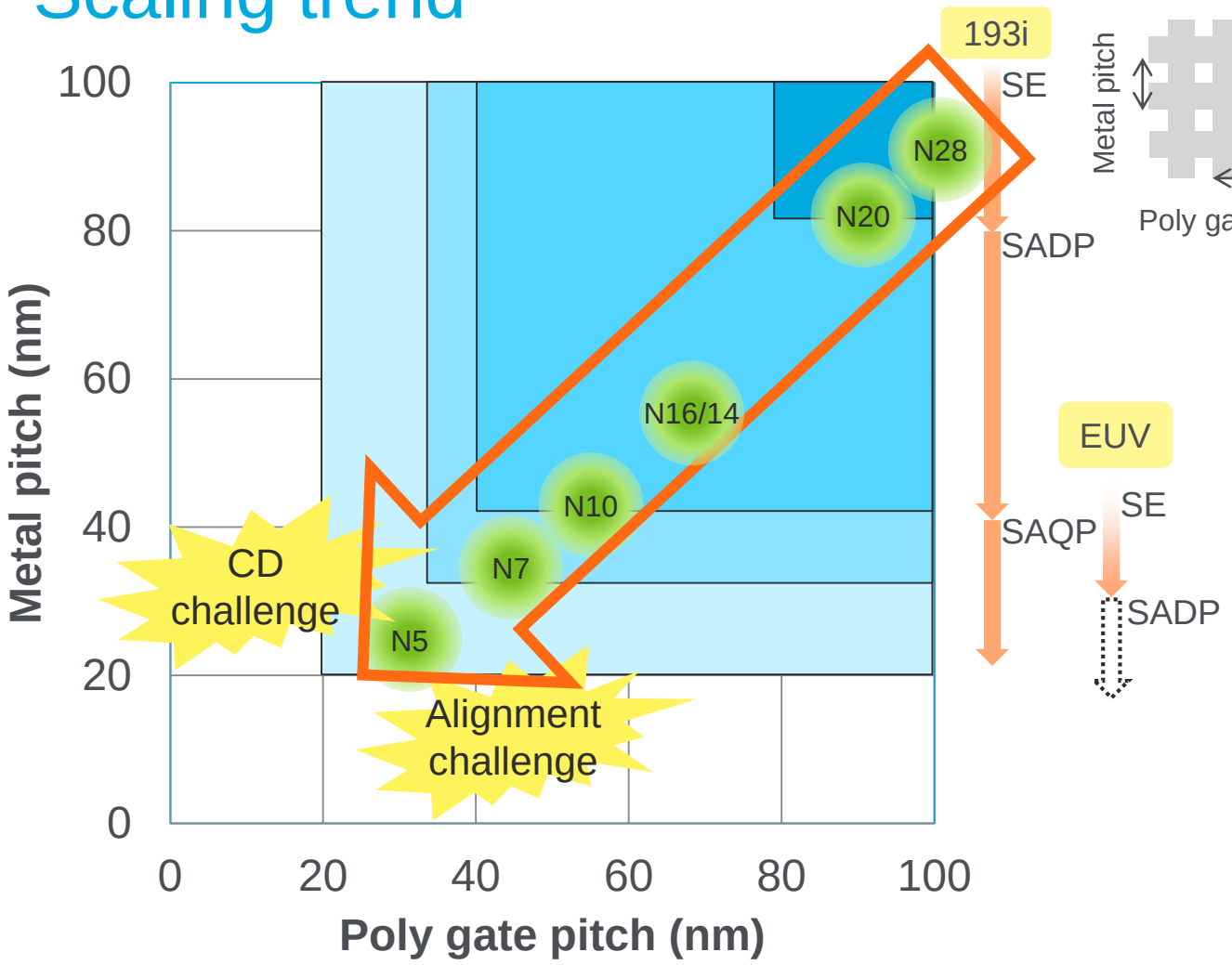
Technology trends

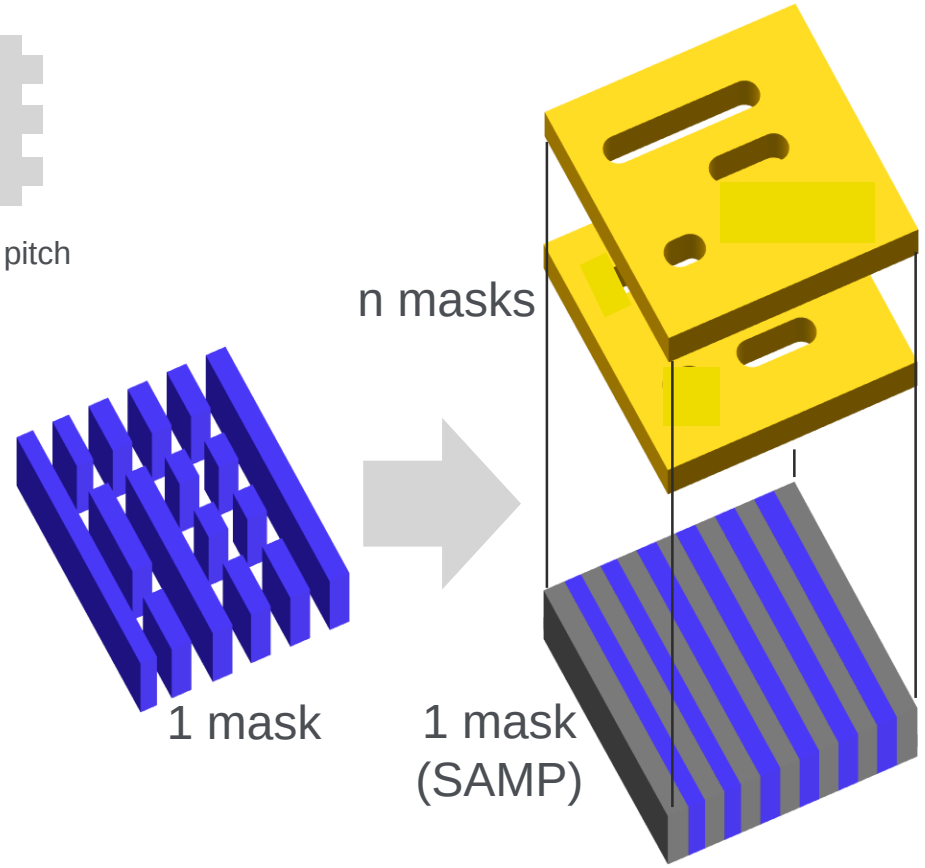
Technology trend



Vertical utilization is the key approach towards sub-10nm generation

Scaling trend

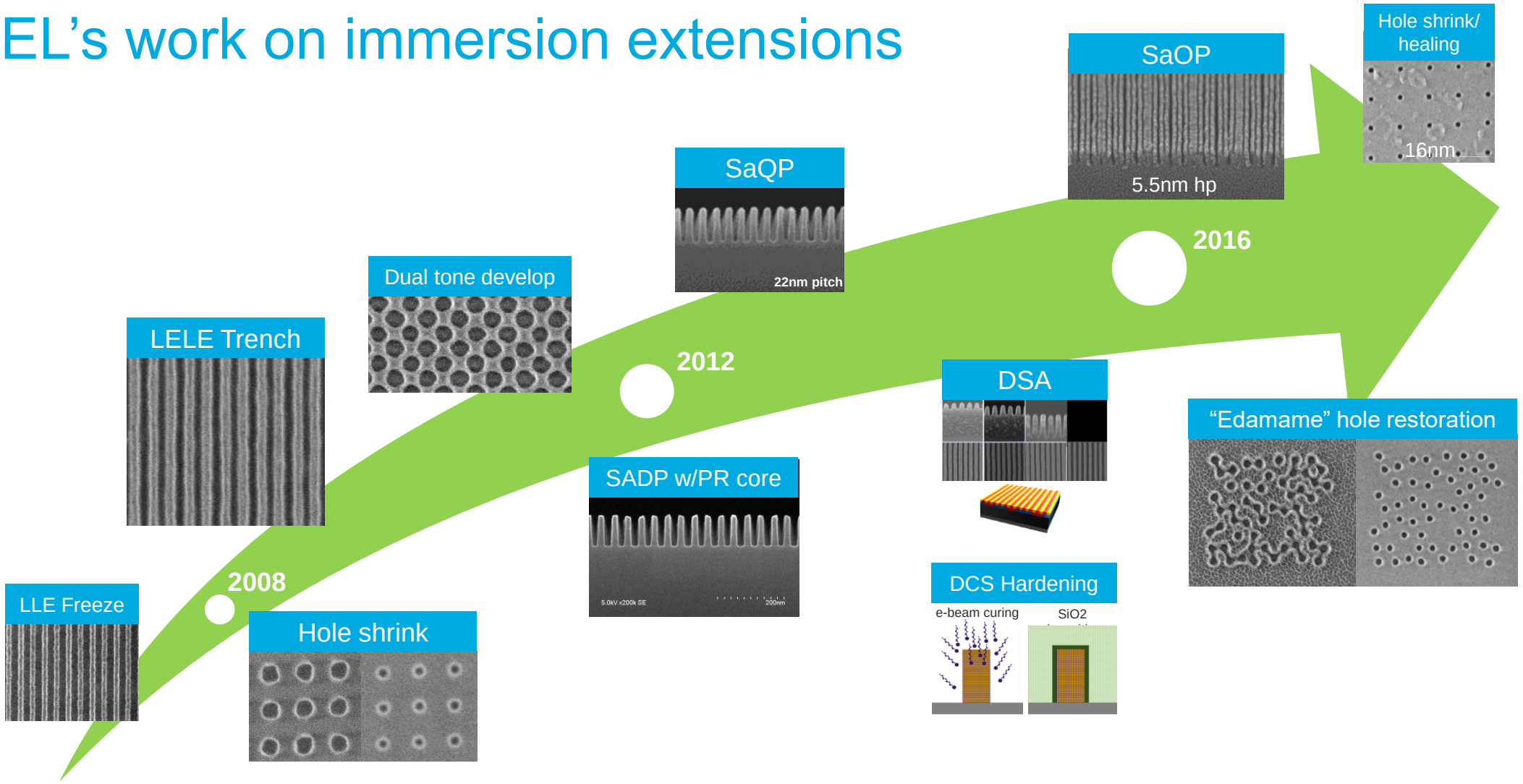




Design layout change from 2D to 1D

Complex and fine patterning technology is required for further scaling

TEL's work on immersion extensions

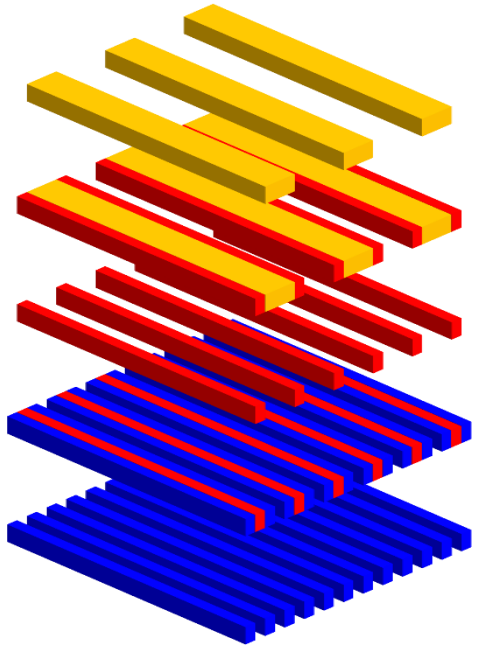


TEL has been contributing to develop evolutional patterning technologies

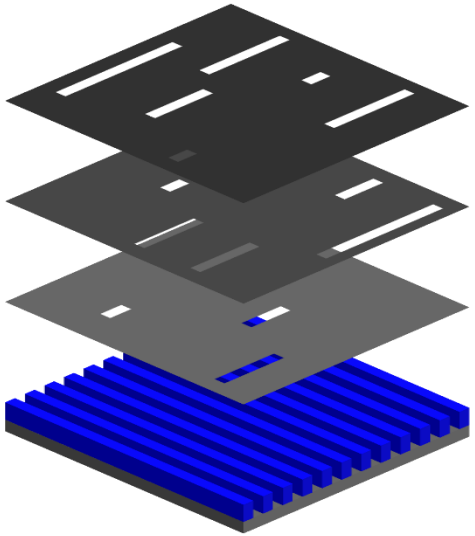
Patterning challenges and approach

Patterning challenges to EPE

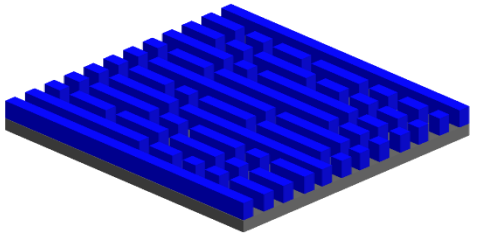
SAQP



Line cutting with LELELE



Final pattern



$$EPE = f(\text{CD variation}, \text{Pattern OL})$$

Mandrel, spacer, cuts
Traditional sources of CD variation
Roughness

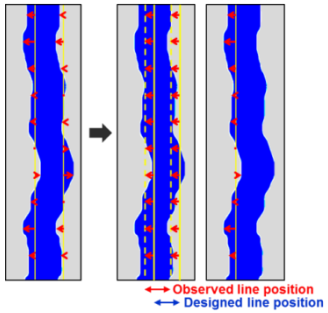
Previous pattern
Cuts to the grid
Cuts to each other

(EPE: Edge Placement Error)

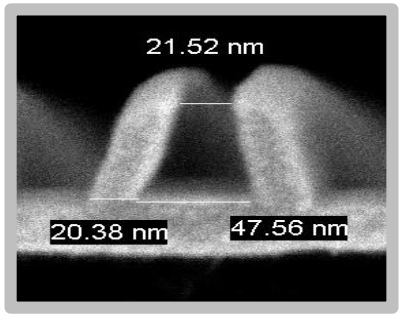
EPE control is critical for further extension

Various challenges

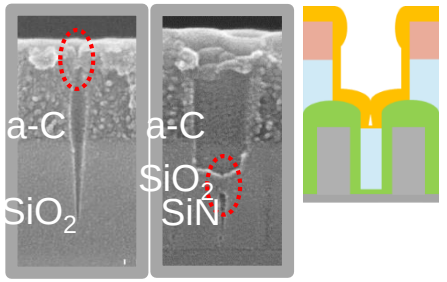
CD Variation



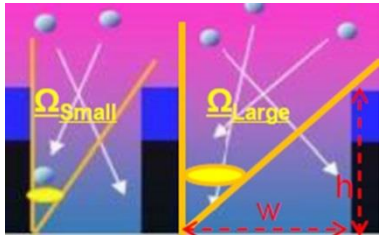
Line roughness (LER/LWR)



Pattern profile (leaning)



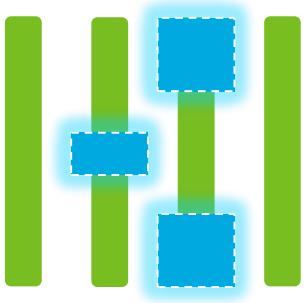
Etch clogging



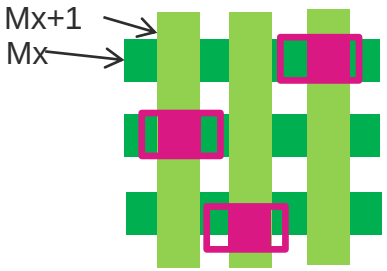
(N. Kuboi et al, J Vac. Sci. Technol. A 31 (6), Nov/Dec 2013)

Loading effect

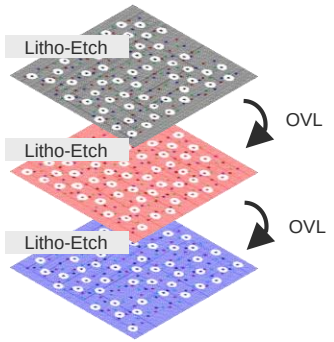
Overlay



Alignment of cut/block to grid



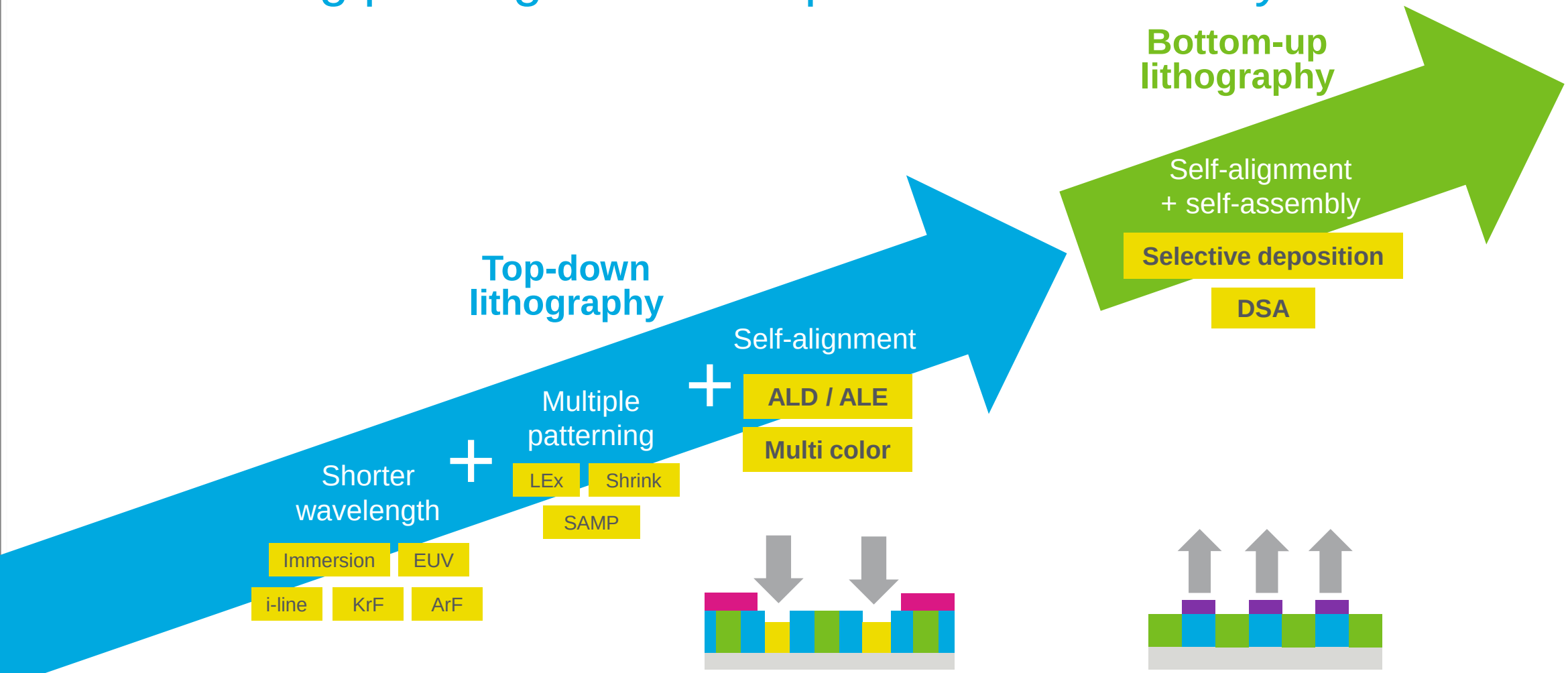
Alignment of via to metal lines



Alignment of holes at multiple LE

Numerous factors impact EPE

Patterning paradigm towards placement accuracy



The paradigm is expanding to self-alignment and bottom up approach

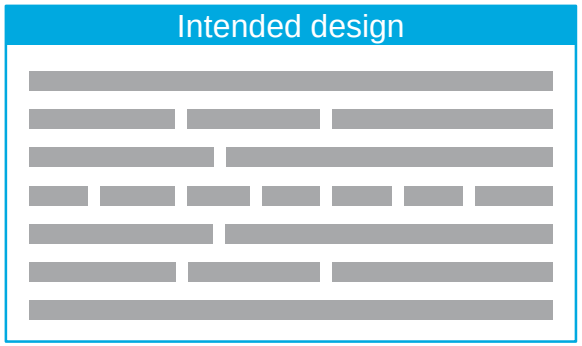
Patterning challenges and approaches

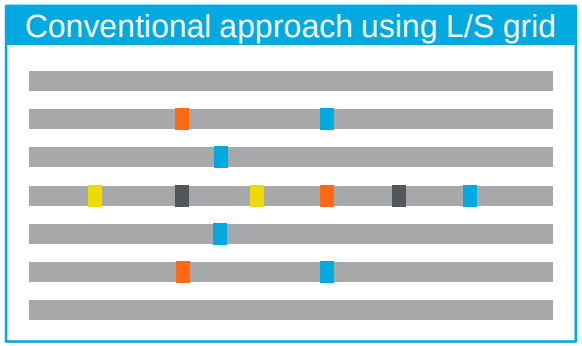
	Typical scheme	Challenge	Potential approach
Grid formation	SADP SAQP	LER, LWR, local CDU	▪ Etch smoothing (DCS) ▪ Spacer reshape
		Spacer leaning	▪ Dep / cure and trim
		Cost	▪ PR mandrel
Cut / Block	LEx	CD, CDU, CER	▪ Healing, shrink
		Alignment with grid (within layer)	▪ SAB
		Cost and complexity mitigation	▪ EUV
Via formation	LEx	CD, CDU, CER	▪ Healing, shrink
		Alignment with metal lines (inter layers)	▪ FSAV
		Cost and complexity mitigation	▪ EUV
New process development		Atomic level process	▪ ALD / ALE
		Bottom up lithography	▪ Selective deposition

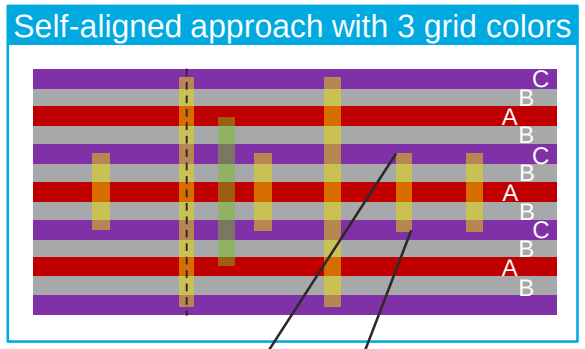
Today's presentation

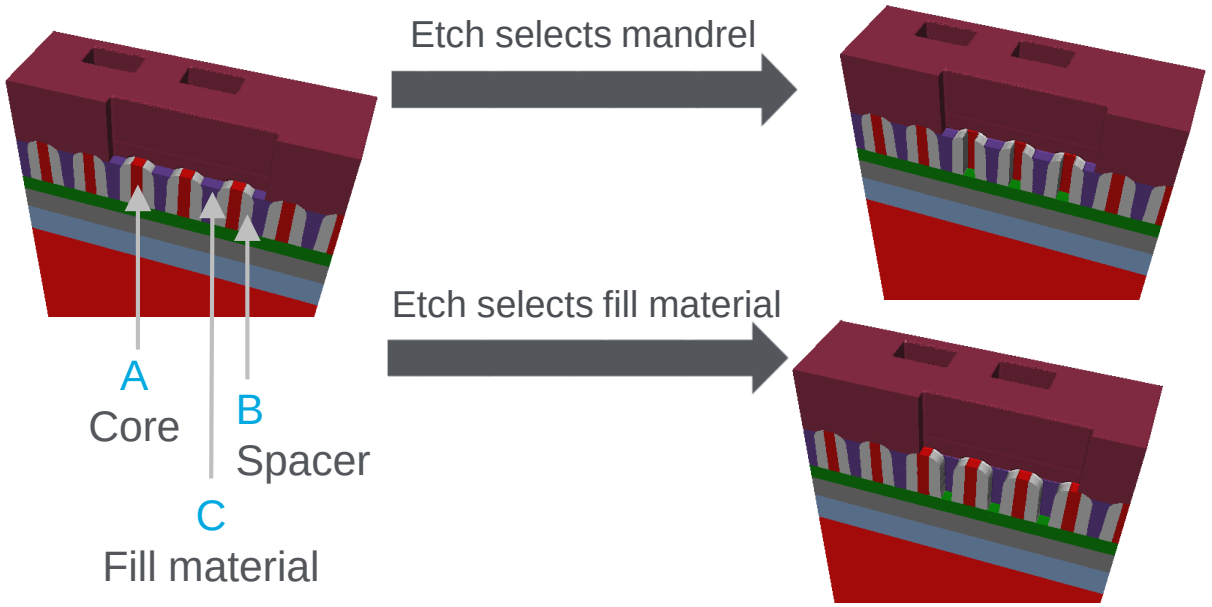
Process technology examples

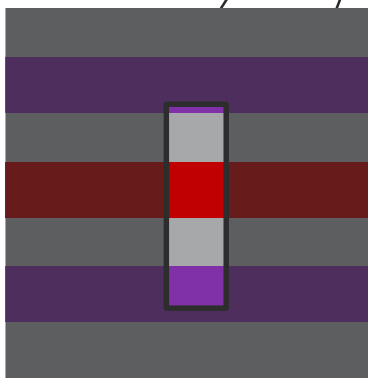
Self-alignment through etch selectivity





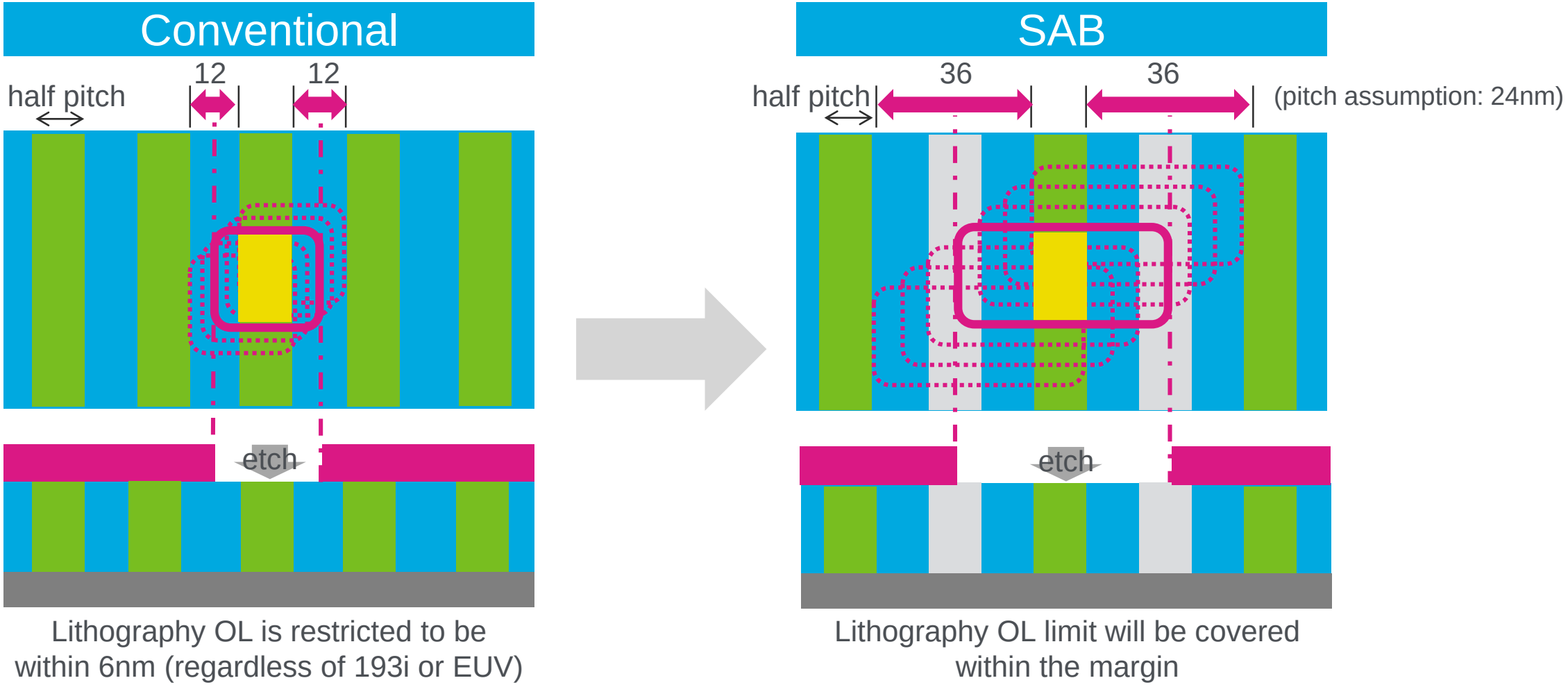






Self-alignment of cut/block is enabled by SAB, using etch selectivity

Placement margin improvement by SAB



Lithography OL is restricted to be within 6nm (regardless of 193i or EUV)

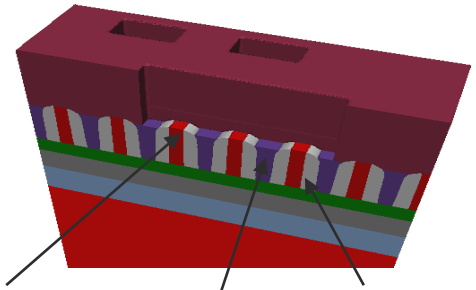
Lithography OL limit will be covered within the margin

Placement margin of hard mask is 3 times relaxed

Flexibility of material selection for SAB

Potential material combinations

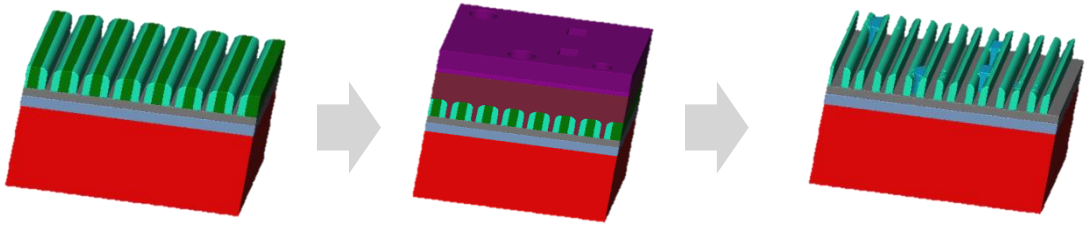
Case #	Mandrel (A)	Spacer (B)	Fill (C)
1	a-Si	MeOx	SOG
2	SiN	Oxide	SOC
3	a-Si	Oxide	SOM

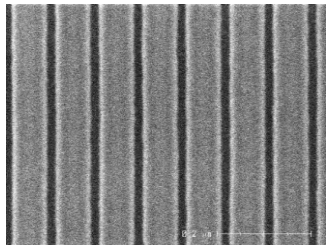


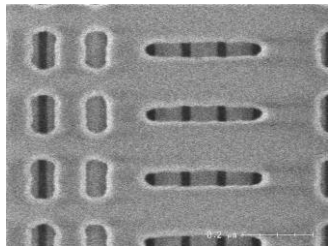
A = Mandrel B = Spacer

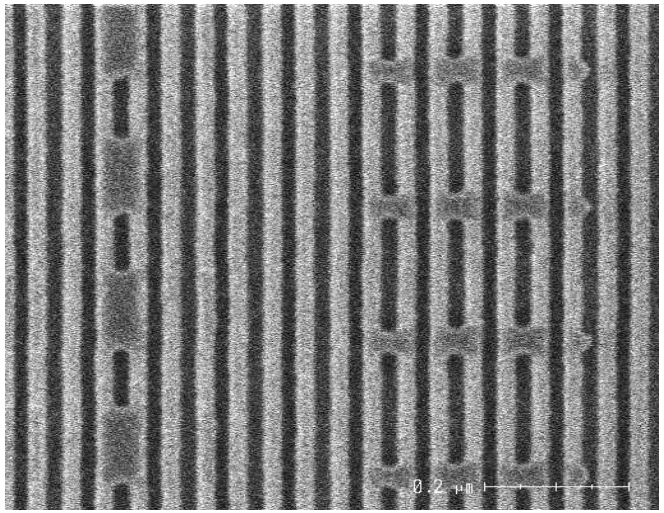
C = Fill material

SAB demonstration (case 2)





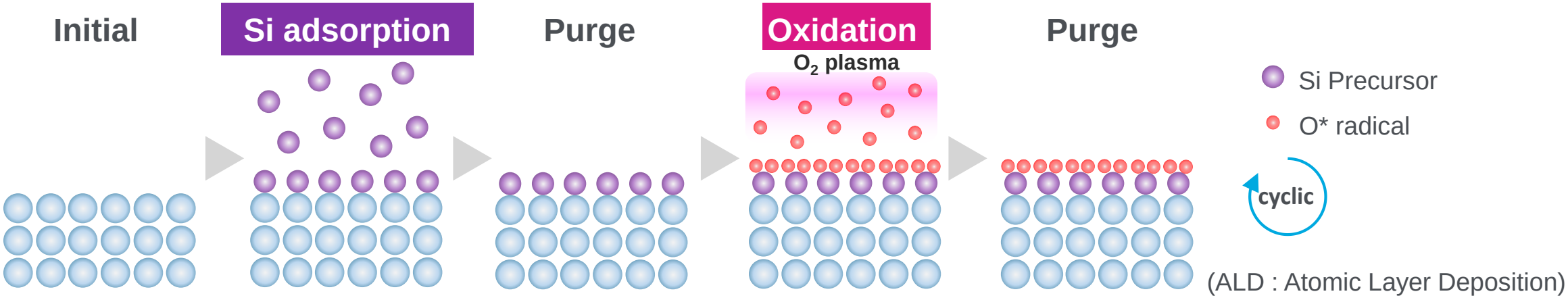




Combination of non-metal materials

Various material combinations can be implemented
Combination of non-metal materials is demonstrated

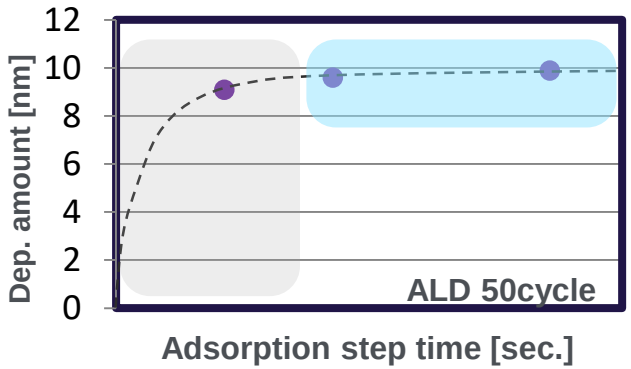
ALD technology (SiOx)



(ALD : Atomic Layer Deposition)

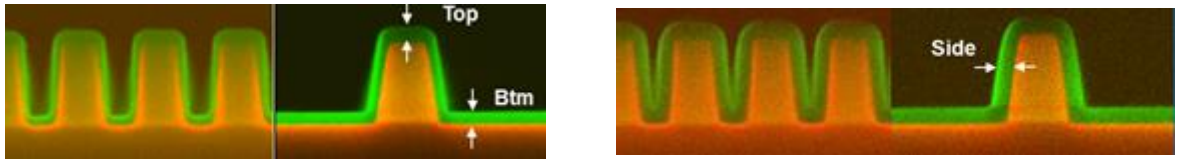
Self-limited reaction

(0.2nm / cycle)



Film coverage comparison

Conventional (CVD) ALD

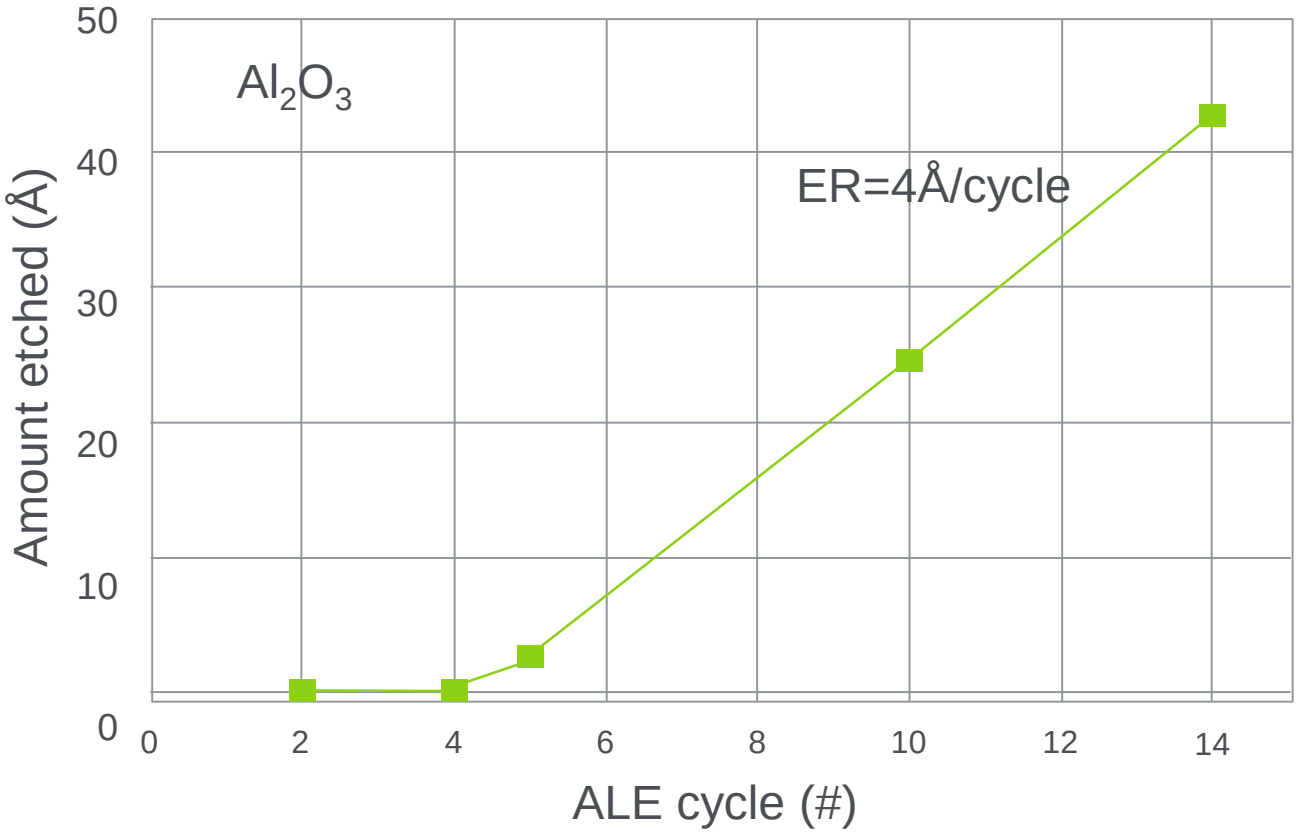


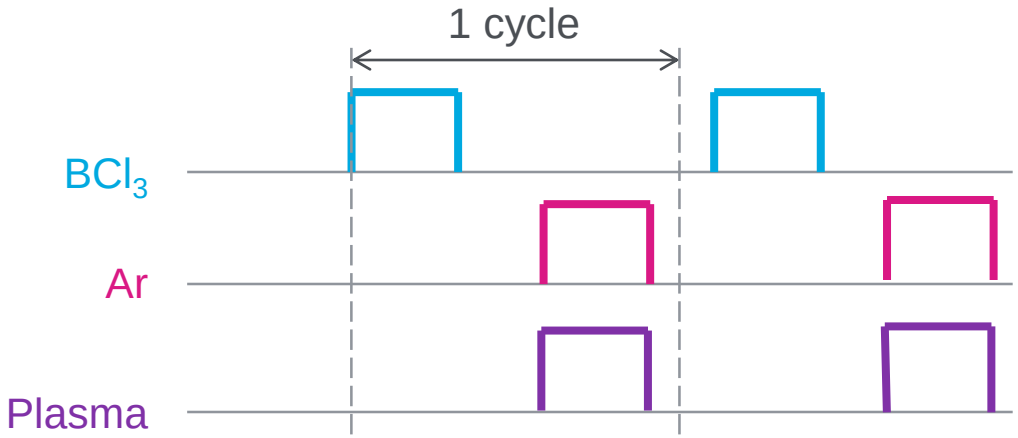
18/8/13nm 18/12/16nm 18/17/18nm 18/18/18nm

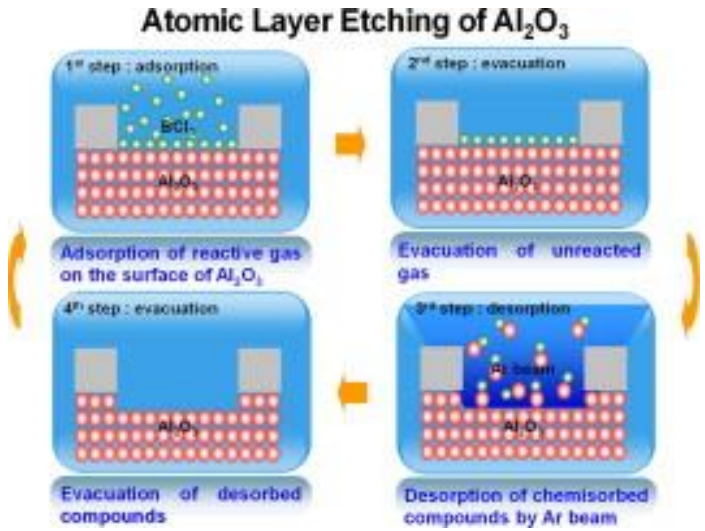
(ΔTop / ΔSide / ΔBtm)

Uniform film coverage by ALD using self-limited half reactions

ALE technology (AlOx)



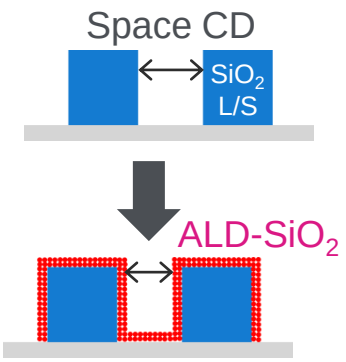




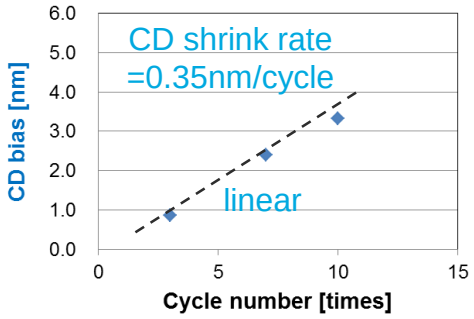
Min *Microelectronic Eng.* 110 (**2013**) 457–460

Anisotropic quasi-ALE of AlOx by self-limited half reactions

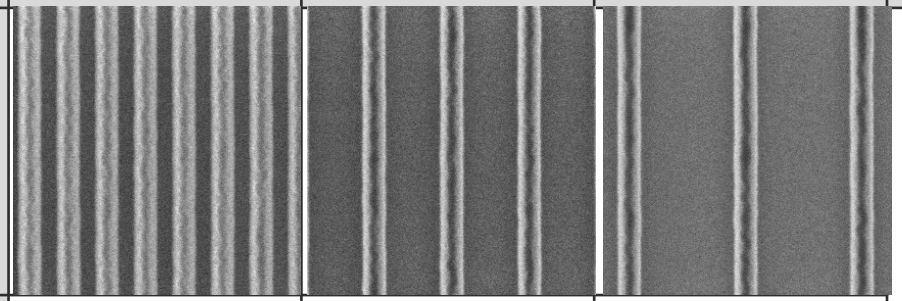
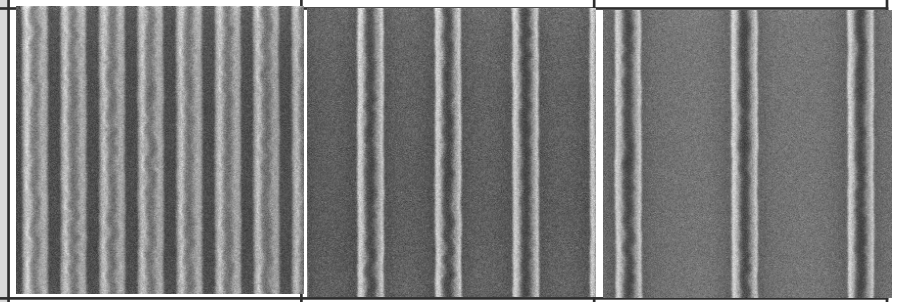
ALD CD shrink



CD shrink mechanism

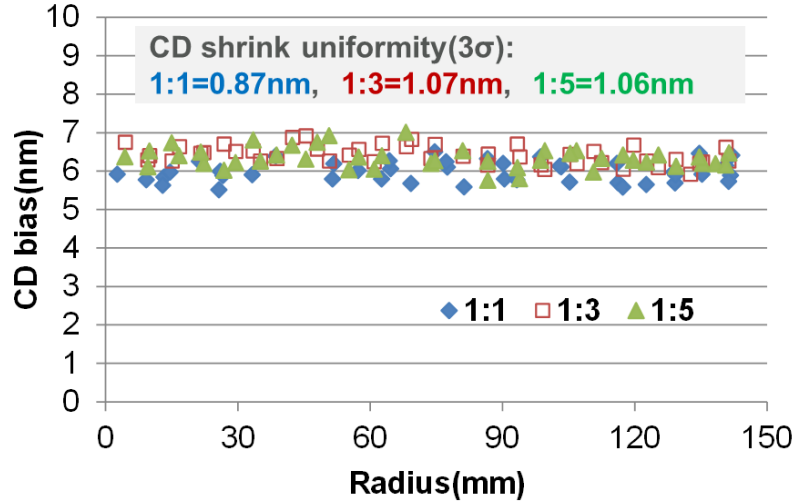


Controllability

L : S	1:1	1:3	1:5
Initial			
Line CD	47.67nm	50.83nm	50.76nm
Post ALD			
Line CD	53.61nm	57.27nm	57.15nm
CD bias	**5.98nm**	**6.41nm**	**6.30nm**

Pattern density impact

CD shrink uniformity across wafer



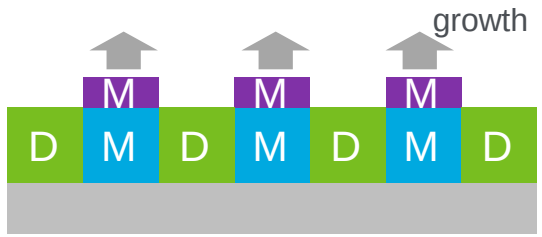
→ CD loading by density : 0.43nm

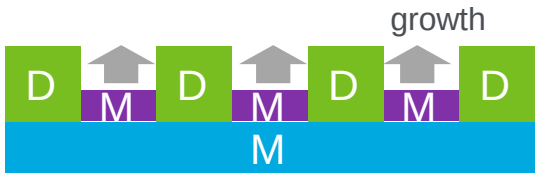
Uniform CD shrink without CD loading is achieved

Bottom-up lithography

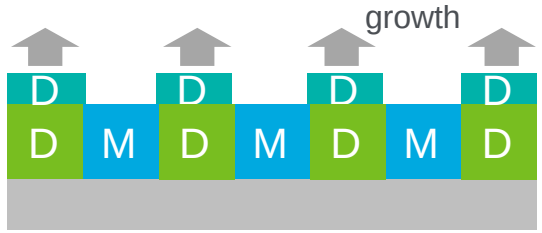
Selective deposition

Metal on metal





Dielectric on Dielectric



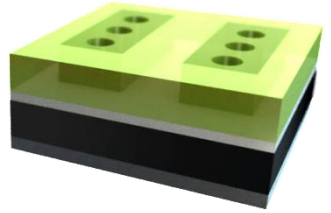
D : Dielectric
M : Metal

DSA

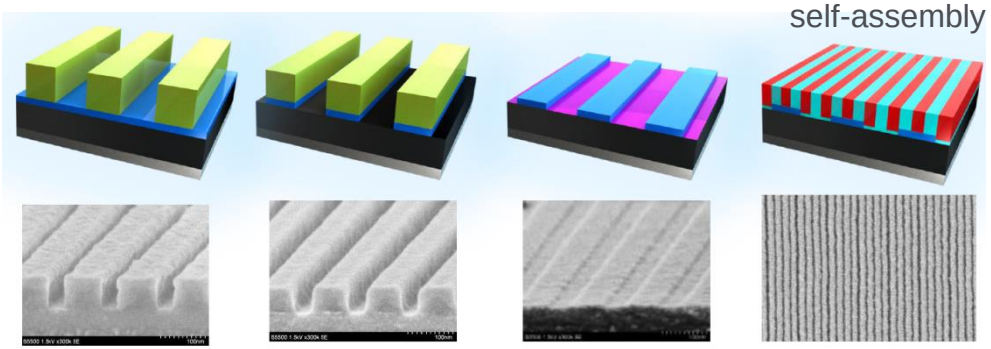
L/S pitch multiplication

x4 multiplication
capable at 30nm pitch

Hole pitch multiplication



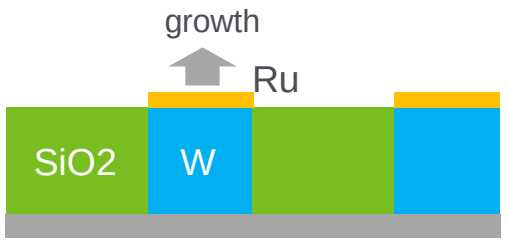
x3 multiplication
capable at 30nm pitch

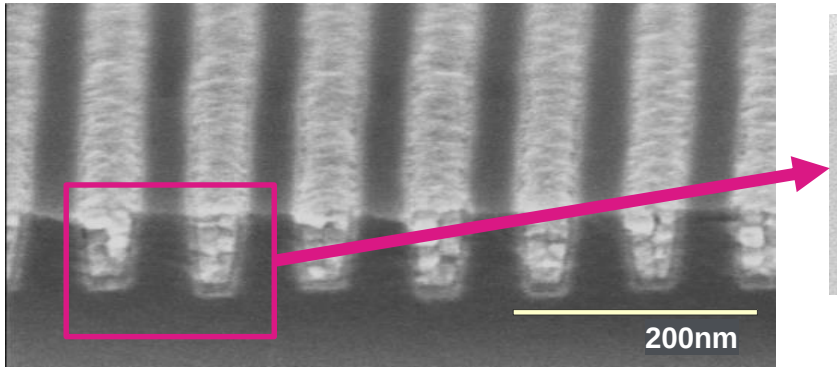


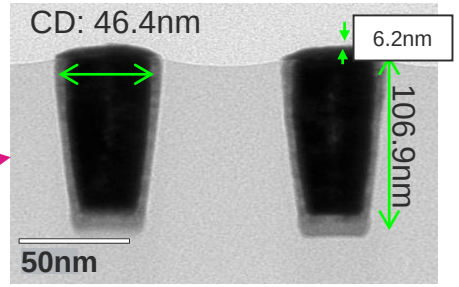
DSA : Directed Self-Assembly

Bottom-up lithography is enabled by self-alignment and self-assembly

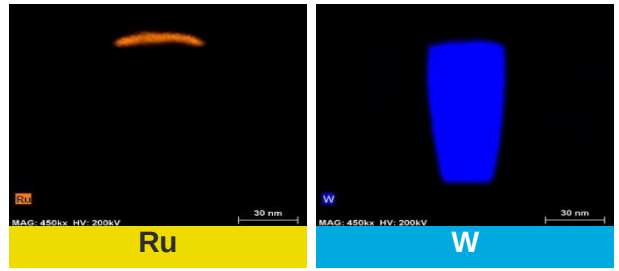
Selective deposition: Metal on metal



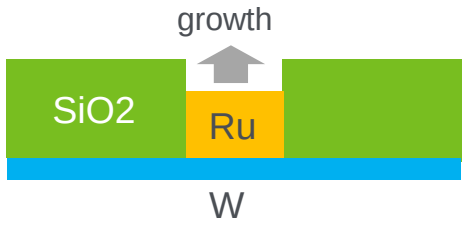


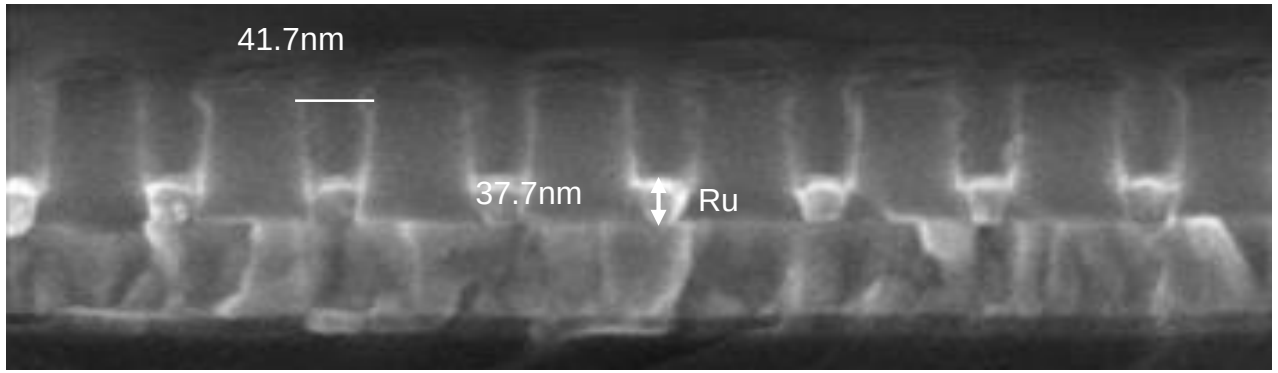


X-TEM

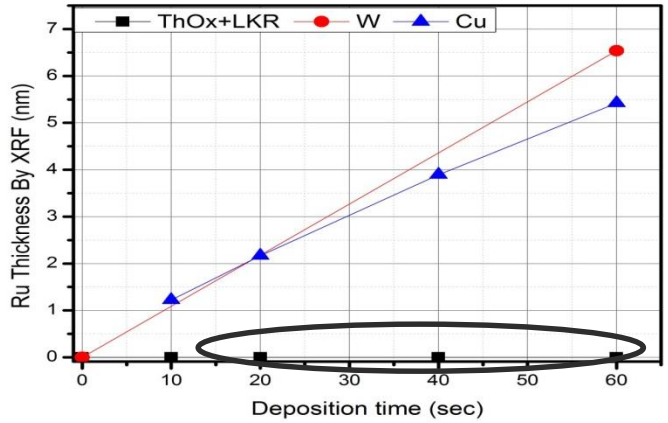


EDX mapping



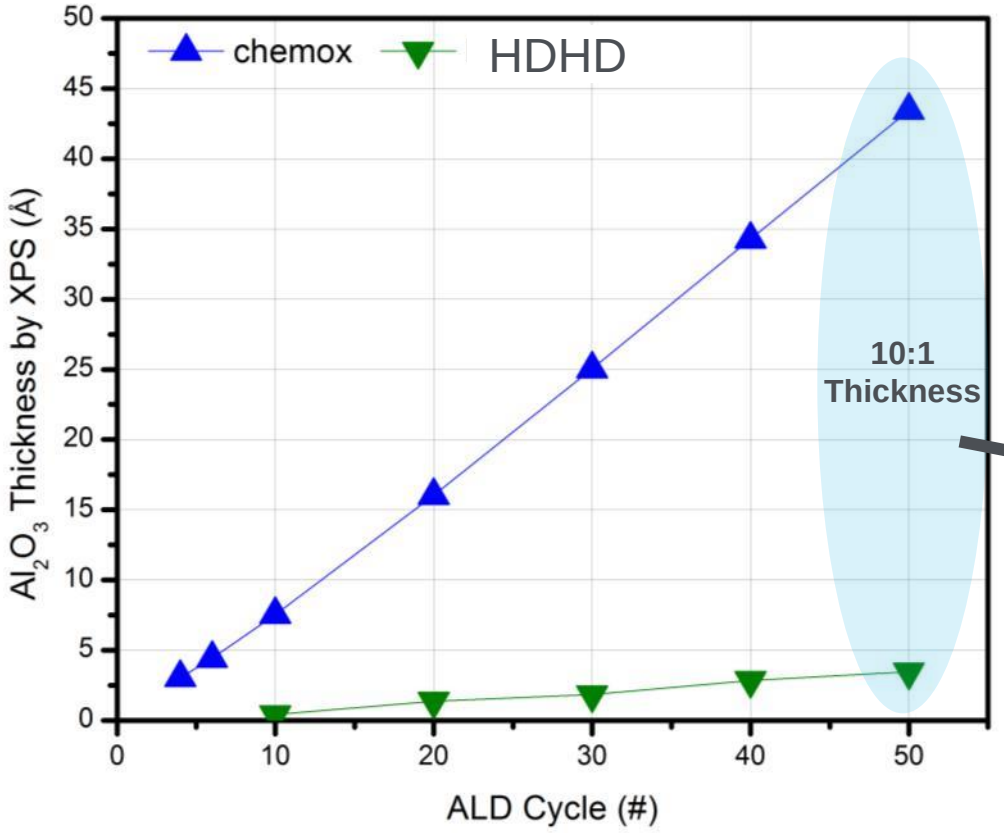


K. Tapily, AVS Focus Topic Selective Deposition, San Jose 2015



Deposition of Ru is demonstrated to grow on W only

Selective deposition: Dielectric on dielectric



K. Tapily, AVS Focus Topic Selective Deposition, San Jose 2015

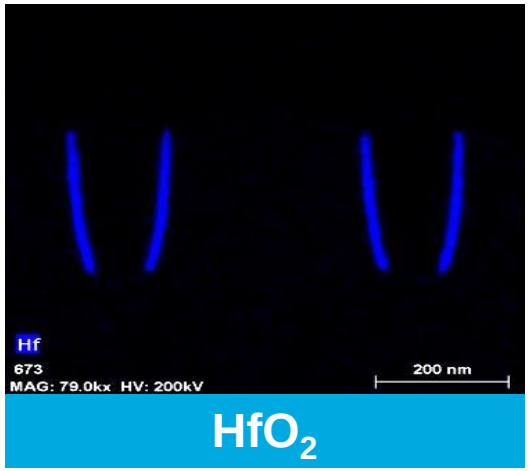
Si substrate treatment:

- HDHD: Cyclical deposition and low-temperature plasma hydrogen (SPA H) treatment
  - Sustained H-termination on Si
  - Delayed ALD Al_2O_3 incubation

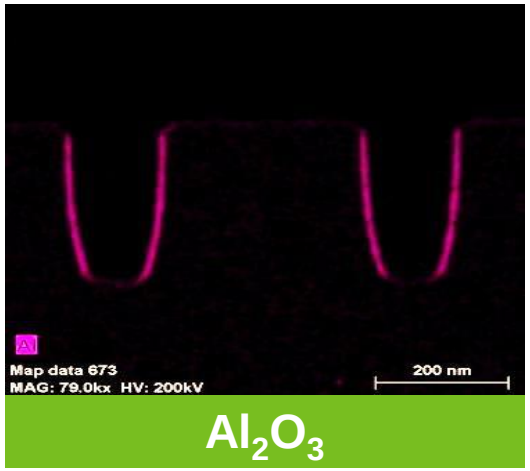
4-5nm selectivity

SPA H plasma is effective in suppressing Al_2O_3 growth up to ~5nm on Si and not on oxides

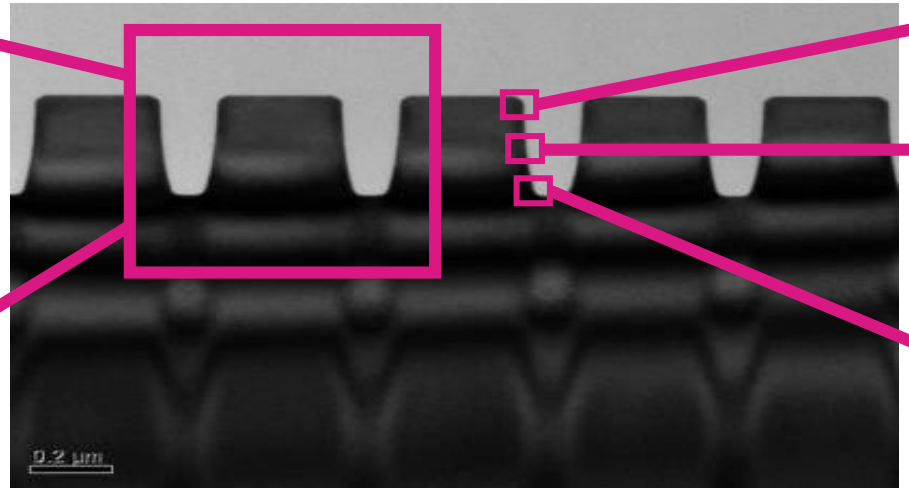
Area selective deposition by combining ALD and ALE



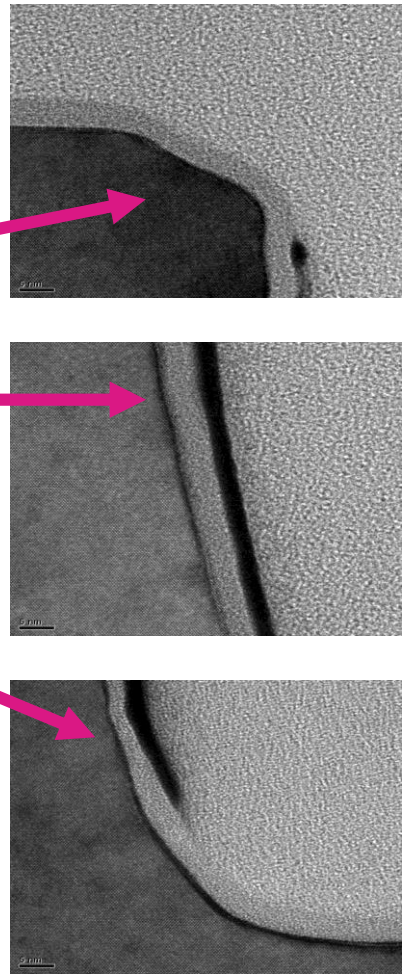
HfO_2



Al_2O_3



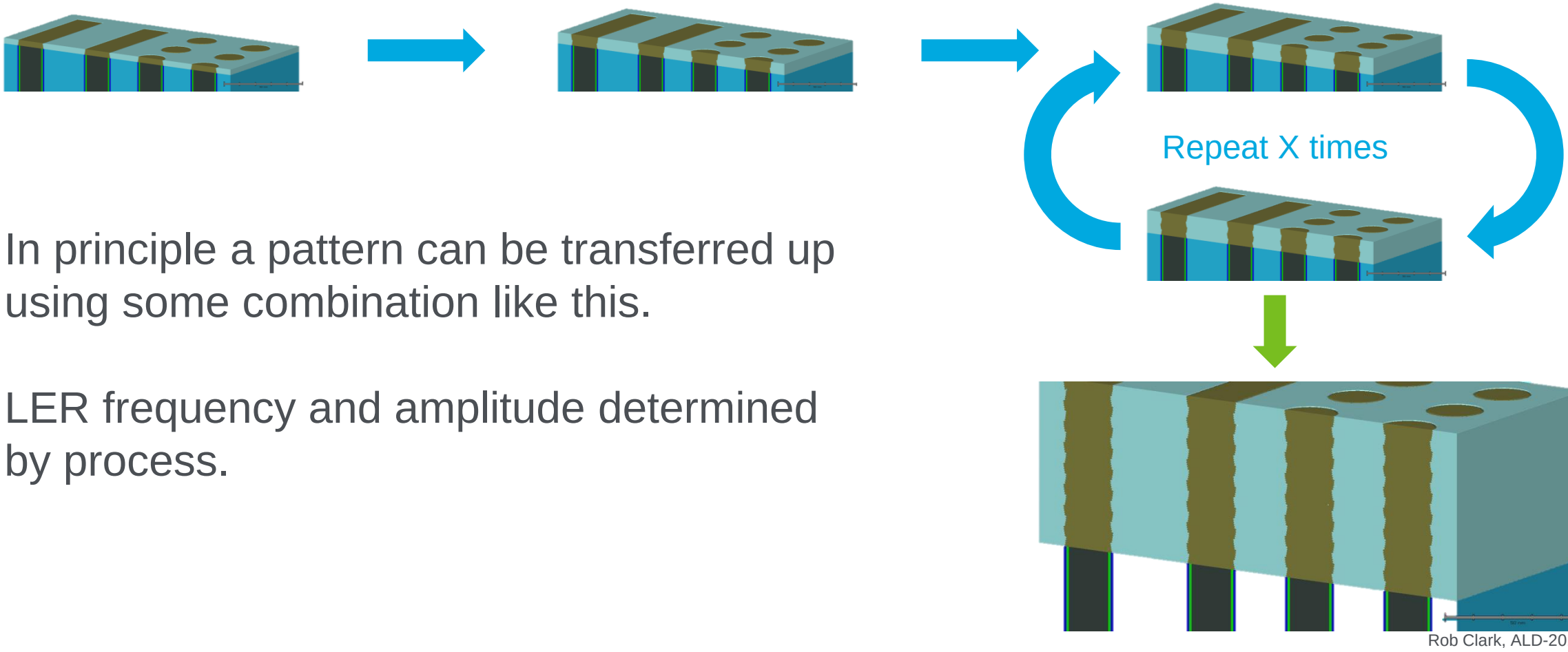
K. Tapily, AVS Focus Topic Selective Deposition, San Jose 2015



Note: Very good selectivity to SiO_2

ALD high K dielectrics followed by anisotropic ALE enables thin ALD sidewall spacers

Principal of pattern transfer with selective dep



In principle a pattern can be transferred up using some combination like this.

LER frequency and amplitude determined by process.

Rob Clark, ALD-2016

Pie in the sky for now, but more and more selective processes will be needed going forward

Summary

Summary

- 3D architecture and scaling are key requirements for sub 10nm generation
- EPE is the fundamental challenge for advanced patterning
- Patterning paradigm is expanding to self-alignment and bottom up approach
- TEL will continuously contribute to achieve evolutional patterning technology

Patterning tool portfolio

TELINDY PLUS

NT333™

Triase+™

CLEAN TRACK™ LITHIUS Pro™ Z

Tactras™ Vigus™

Certas LEAGA™

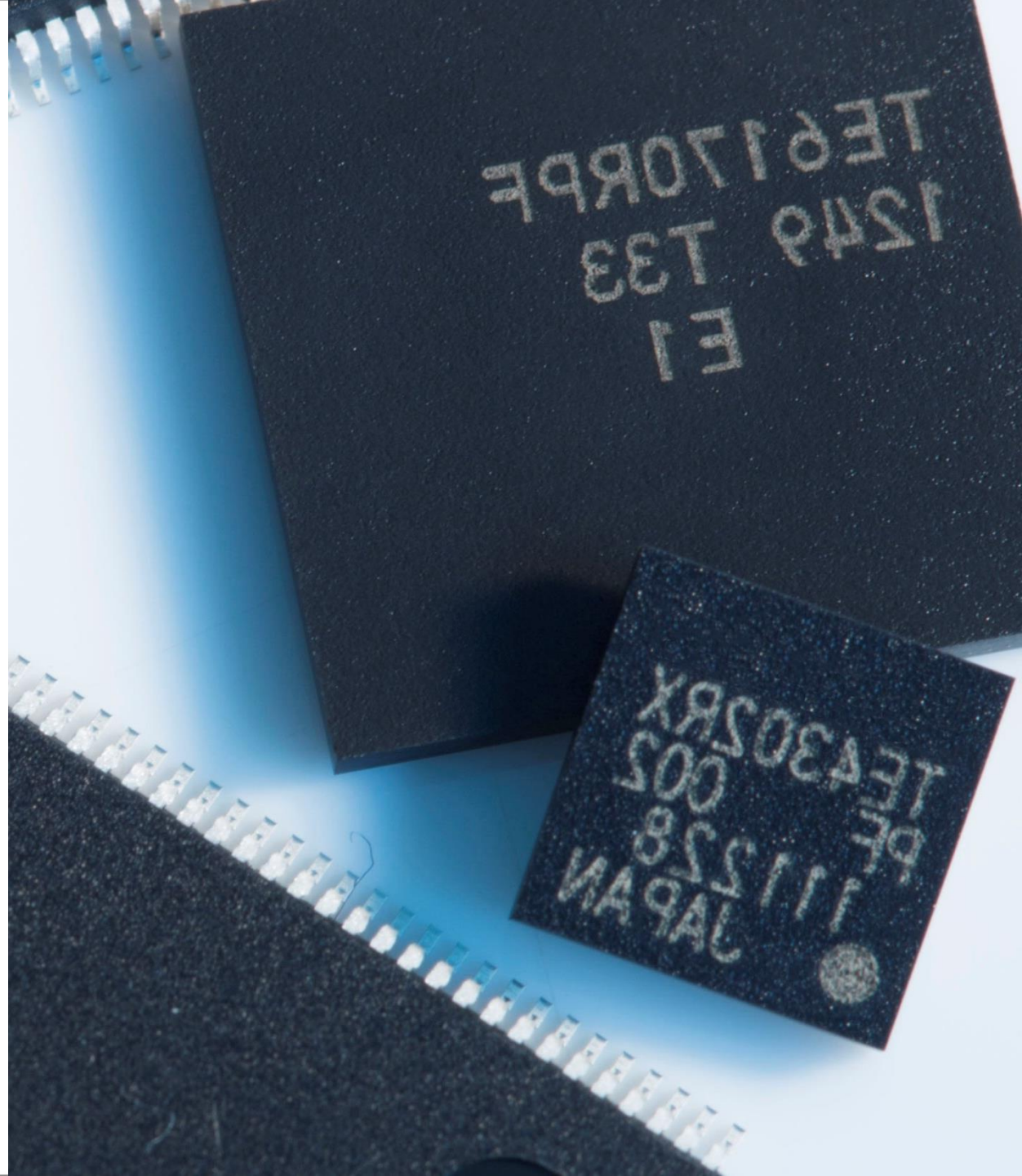
CELLESTA™ -i

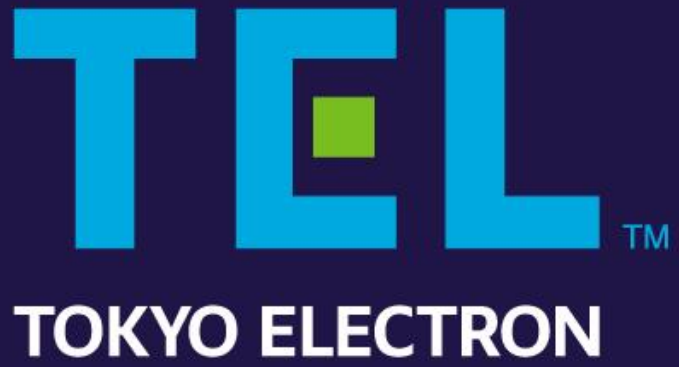
NS300Z

Acknowledgement

- Hidetami Yaegashi[1]
- Masanobu Honda[2]
- Ben Rathsack[3]
- Mark Somervell[3]
- Kanda Tapily[4]
- Kyle Yu[4]
- Rob Clark[4]

[1]Tokyo Electron Limited
[2]Tokyo Electron Miyagi Limited
[3]Tokyo Electron America, Inc.
[4]TEL Technology Center, America, LLC

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