IBM Semiconductor Technology Research - Albany

Selective Metal Deposition for nano device fabrication

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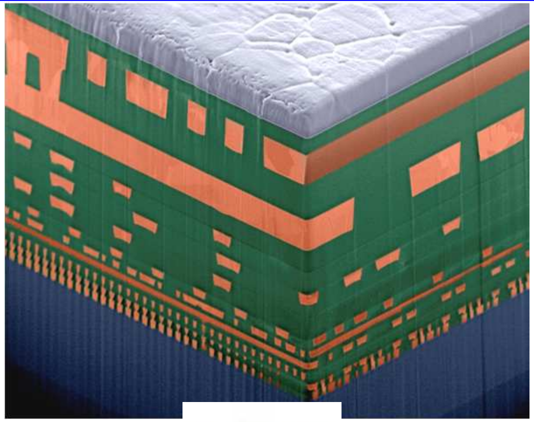
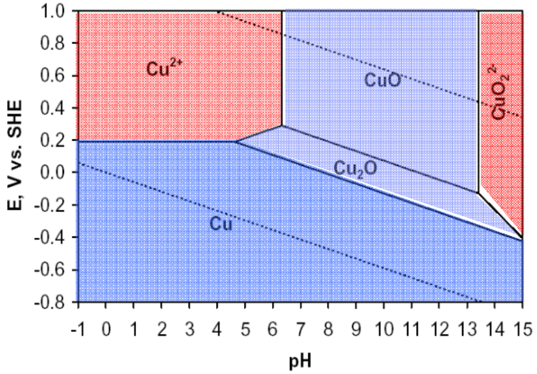
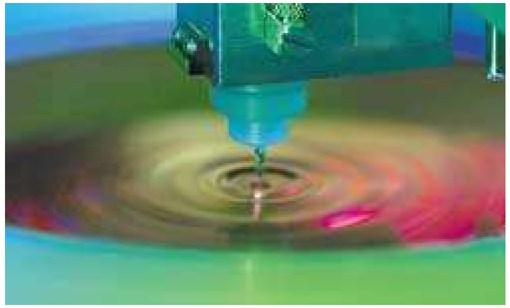
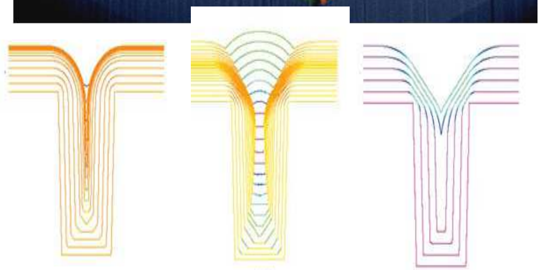
This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities

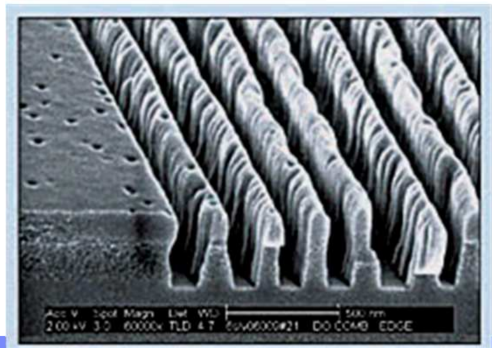
Nano Copper Low K Interconnect BEOL Research: Unit Processing

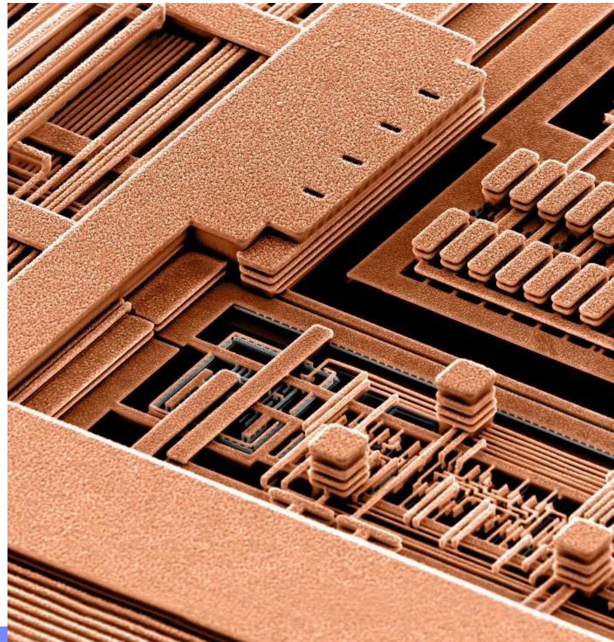


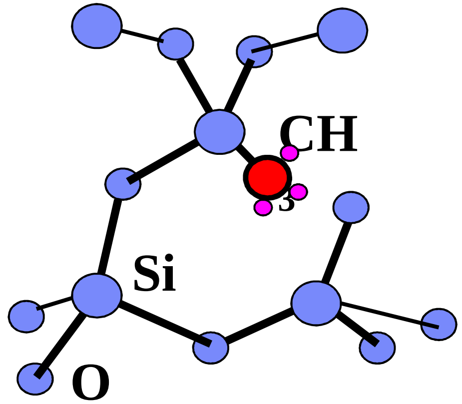


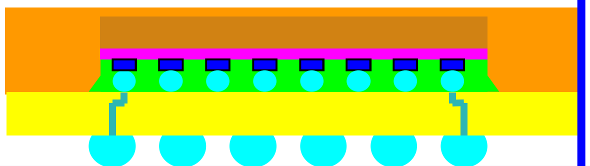












Outline

- **Introduction**

  - **Cu-Low k interconnect reliability enhancement with metal cap.**

  - **Selective CVD Metal Deposition technology.**

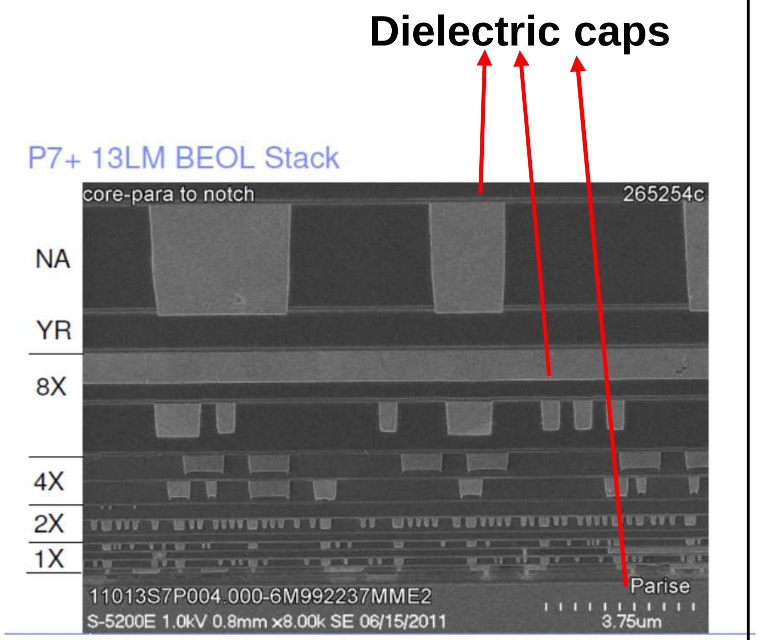
- **Selective metal deposition processes : Co, Ru, Mn**

- **Selective Co Deposition application in device fabrication**

- **Summary**

- **Acknowledgments: This work was performed at various IBM Research and Development Facilities. This review also included contributions of numerous members of IBM metal teams , PFA, unit processes, equipment vendors and universities. The contribution are acknowledged.**

Cu Barrier Cap in IBM's 32 nm (90 nm pitch) Cu-low k interconnect



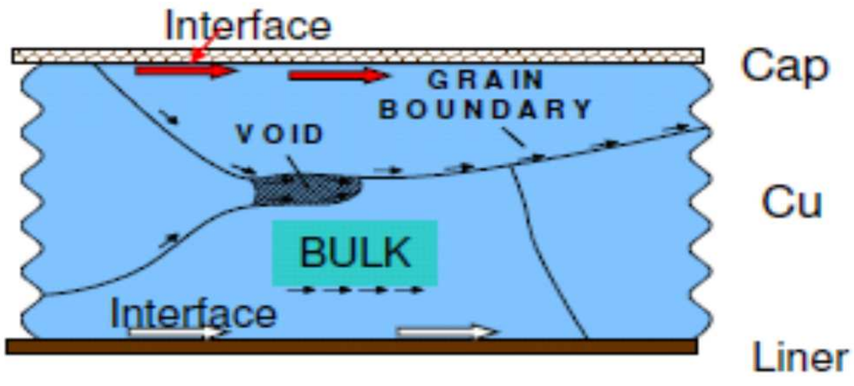
- **Prevent inter/intra level Cu diffusion into ILD dielectrics**
- **MUST shut down Cu diffusivity at top surface for EM reliability**
- **Act as a barrier to humidity ingress**
- **Act as an etch and CMP stop layer**
- **Good electrical properties with high breakdown to provide chamfer benefit**
- **Stress balance at the Cu low-k interconnect interface**
  - Preferable cap with compressive stress to compensate for tensile stresses in ILD
- **Good conformality to fill Cu divots**
- **Minimize impact on BEOL capacitance**

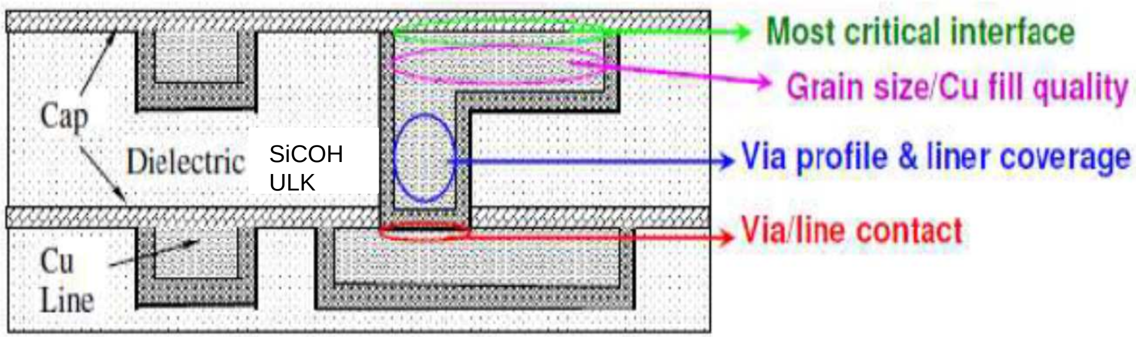
Contribution to interconnect capacitance becomes important as device dimension decreases

→ **SiN (k=7) was replaced with SiCNH (k=5.3) at 90 nm node**

Cu-Cap Interface and its Impact on Electromigration

- Activation energies for Cu interconnects
  - bulk diffusion 2.3 eV
  - grain boundary diffusion 1.2 eV
  - interface diffusion 0.7-1.0 eV
- Interface diffusion having lowest activation energy is the fastest diffusion path for copper interconnects

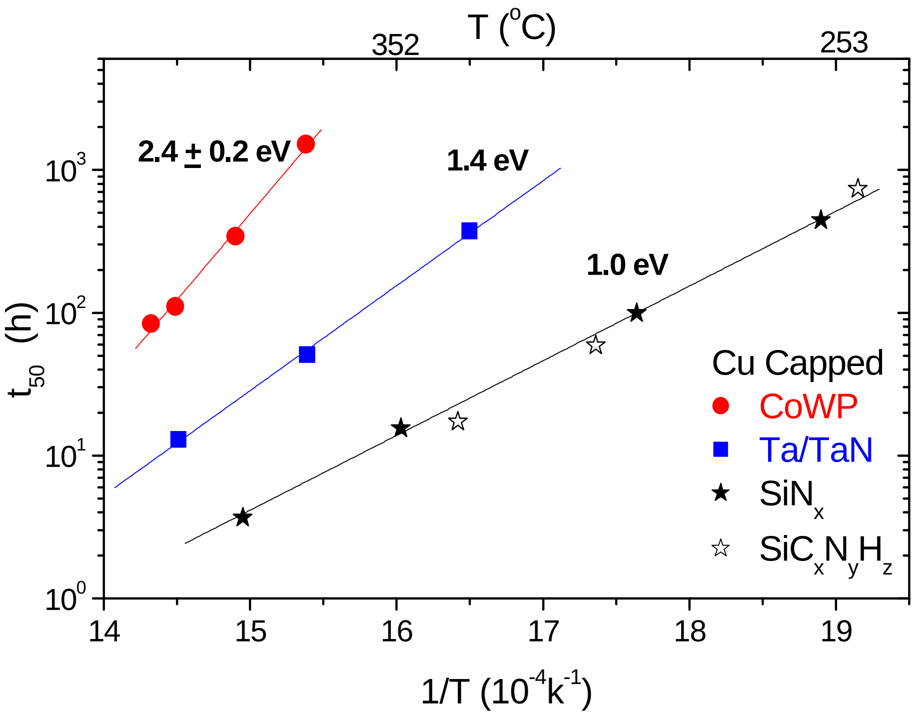


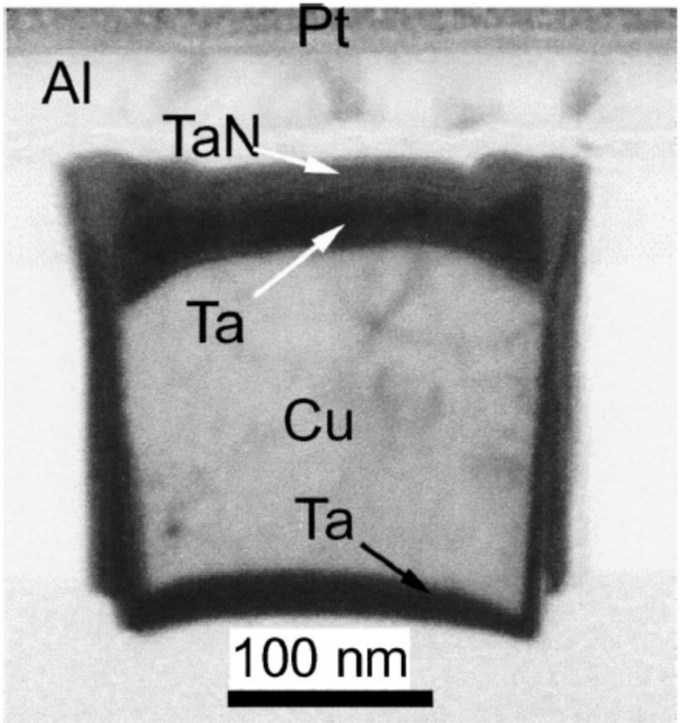


- For damascene integrated copper, the two Cu interfaces are with liner and barrier cap
  - metal liners have good adhesion to Cu
- Better adhesion between the Cu and barrier cap reduces void growth rate and lengthens EM lifetime

ref: Li, et al., Microelectronics Reliability, 44, 365 (2004).

Metal Caps Improved Electromigration Cu-Line Lifetime (CK Hu et al., APL 2003/IRPS 2004)





- Bamboo-like & near bamboo line Cu structure (~250 nm line)

→ **Bulk activation energy** higher with Metal caps (at large dimension)- t_{50} over 1 million years at 100°C, 35 mA/µm^2 for Ta/TaN capped.

→ Thicker Metal Caps with electrochemical deposition (CoWP) or PVD Ta/TaN cap take up Cu volume → increase Cu resistance (for nano Cu dimension)

→ NEED high quality ultrathin (1-5 nm) metal cap for nano Cu interconnect.

Why CVD selective metal cap deposition?

- **Process:**

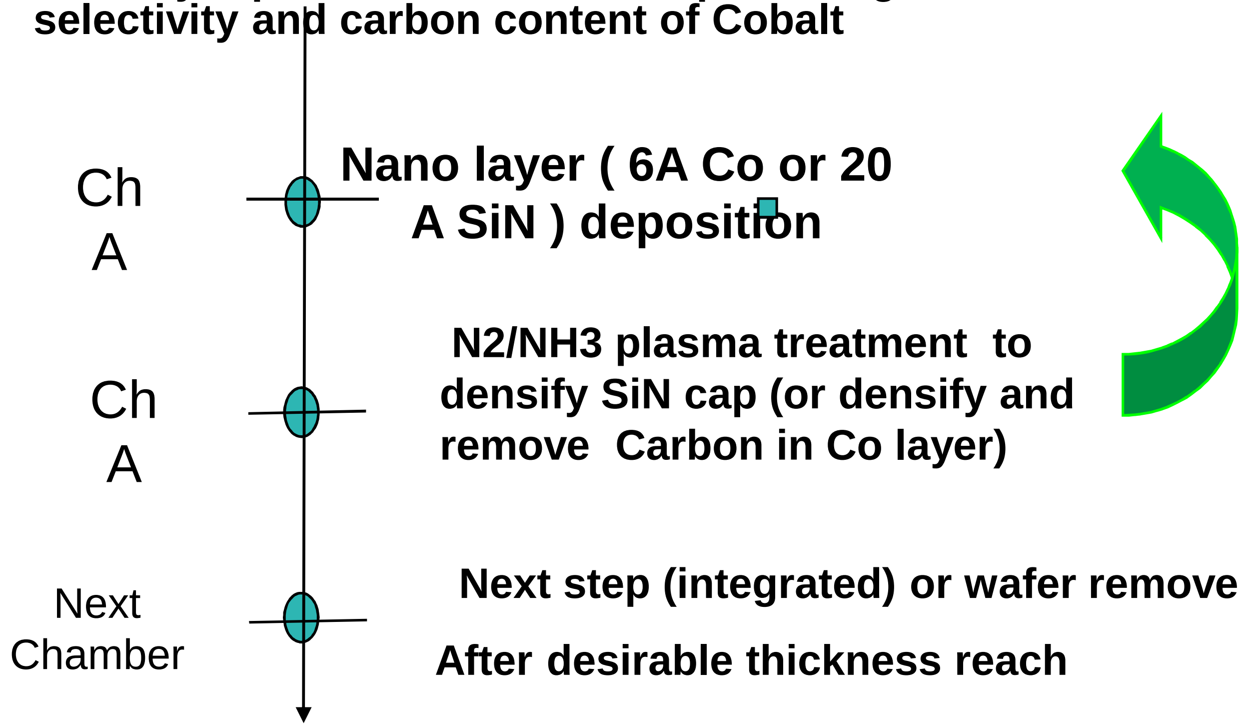
  - **High quality conformal ultrathin (1-5 nm) enabling sub-10 nm Cu interconnect.**
  - **Low defect and compatible to vacuum environment. Low FM. Better thickness control**
  - **Good process reproducibility with low pattern/dimensional sensitivity.**
  - **Can be in-situ integrated with other dielectric CVD in vacuum environment to minimize /eliminated unwanted/uncontrolled metal cap oxidation- enabling thinner metal cap.**
  - **Potentially more friendly to environment: Less chemical use. Volatile CVD precursors can be scrubbed more readily in current fab exhaust system.**

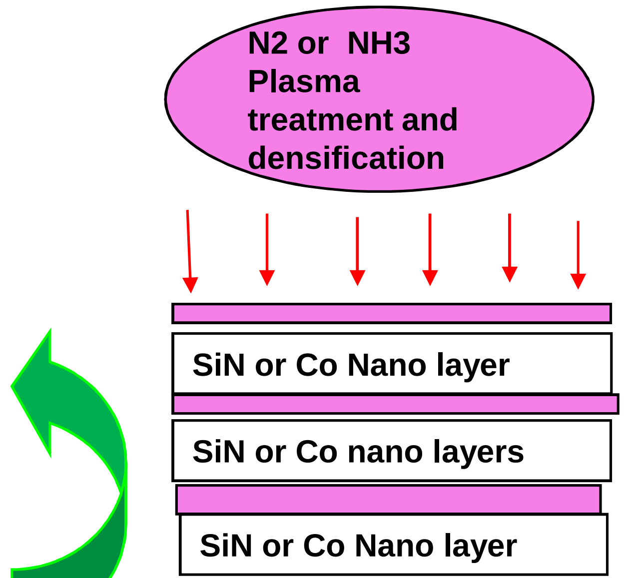
- **Integration:**

  - **No wet chemical or PVD processing minimize the adjacent insulator (ULK) damage or unwanted solvent diffusion into porous ULK (pSiCOH).**
  - **Robust ultra thin metal enable better Cu resistance : Thicker Metal Caps by other process take up Cu volume → increase Cu resistance nano Cu interconnect.**

Cyclic Processes for either nanolayers SiN dielectric or selective Co cap deposition on Cu/pSiCOH ULK

- **Both of SiN and Co Cap deposition deposit by multilayer Cyclic deposition process with either Nitrogen or NH3 treatment steps between each thickness cycle**
- **Nanolayer process improves conformality of SiN.**
- **Nanolayer process enhances step coverage, selectivity and carbon content of Cobalt**





Cyclic process until desirable thickness reach

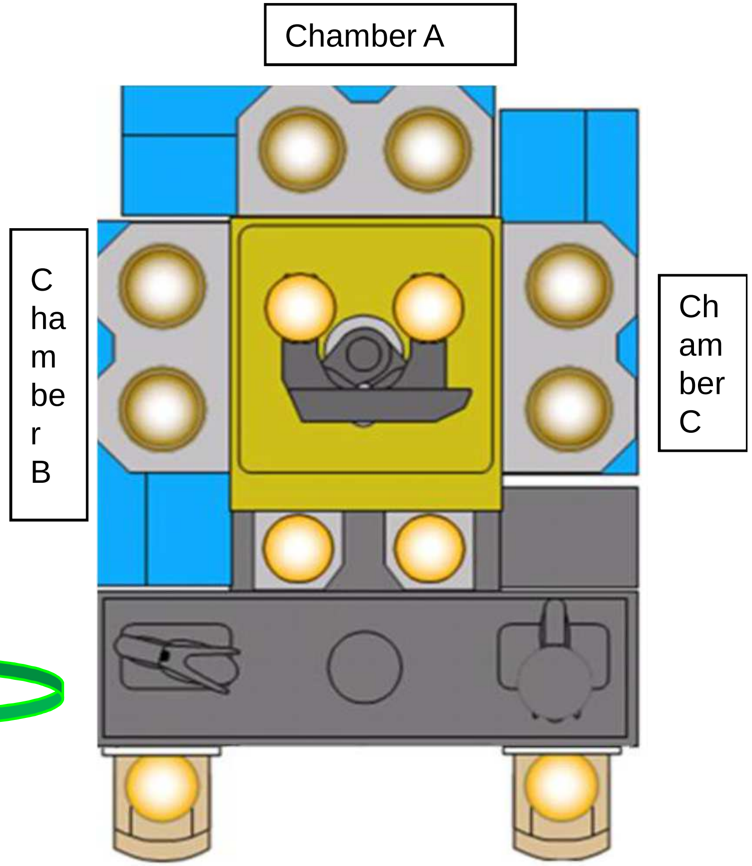
Integrated Cyclic Insitu selective Cobalt and dielectric cap deposition

- **SiH_4 + NH_3 used in Plasma CVD/ALD Nano SiN layer deposition + N_2 plasma treatment at 350 C**
- **Cobalt carbonyl cyclopentadiene precursor is used for selective Co deposition at 210C**

Ch A — **H2 Thermal Preclean of of Cu with Hydrogen**

Ch C — **CVD Co (210 C Thermal H2 PC) followed by cyclic Co dep and NH3 plasma treatment** **damage to ULK**

Ch ChB — **350 C Thermal PC + Dielectric Cap**
- Cyclic conformal multilayer SiN Cap,



ref: Nguyen, et al., Proc. of Intl. Atomic Layer Deposition Conf., pp.124-125 (2013)

Integrated In-situ Selective Co Metal Cap Process (Nguyen et al. ALD 2013)

Plasma treatment step in Selective Co deposition has negative impact to ULK → increase overall C

Selective Co/Dielectrics Cap Process Sequence

Integrated process with NO air-break

Cu surface pre-clean in Ch A

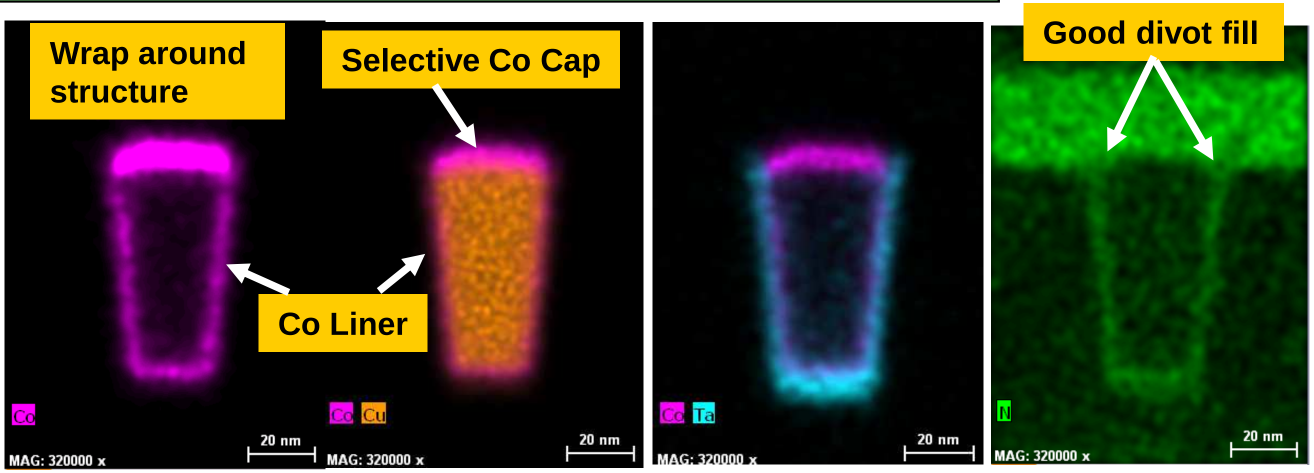
↓

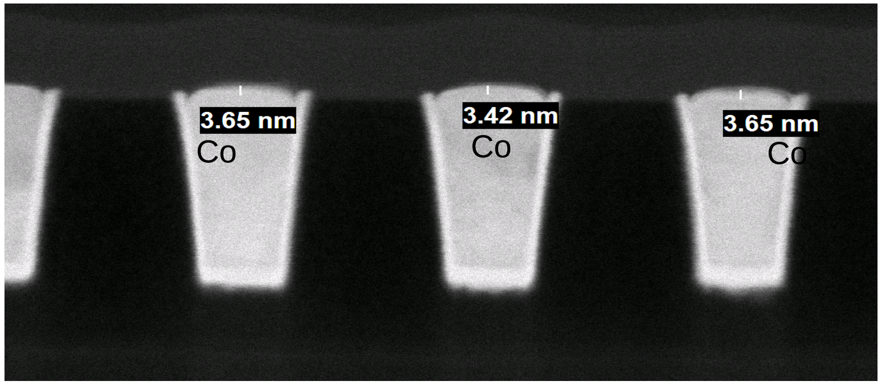
Selective Co metal cap deposition in Ch C (**plasma**)

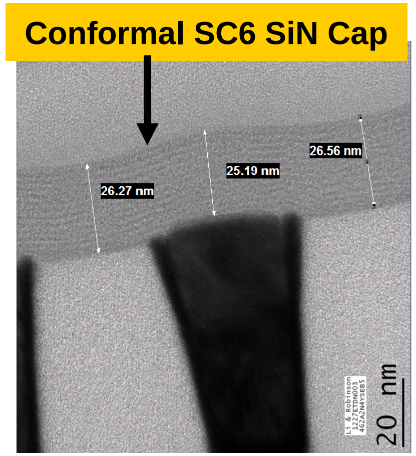
↓

Dielectric barrier cap deposition in Ch A or Ch B

Conformal dielectric barrier film on top of selective Co to fill the divots

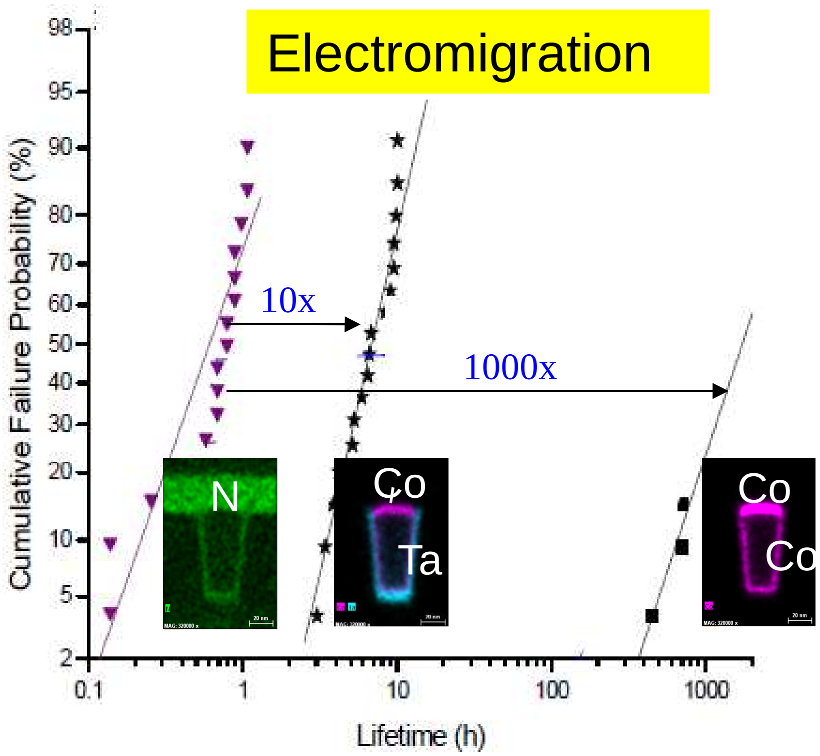


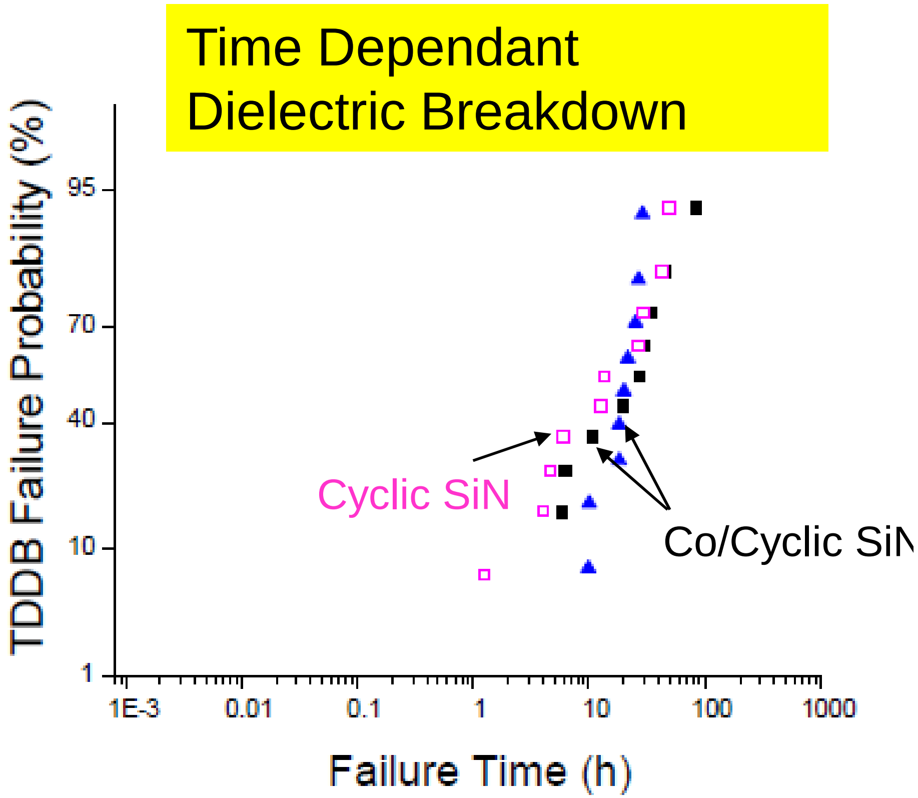




ref: Nguyen, et al., Proc. of Intl. Atomic Layer Deposition Conf., 119 (2013).

EM/TDDB: Integrated in-situ Selective Co/Cyclic SiN



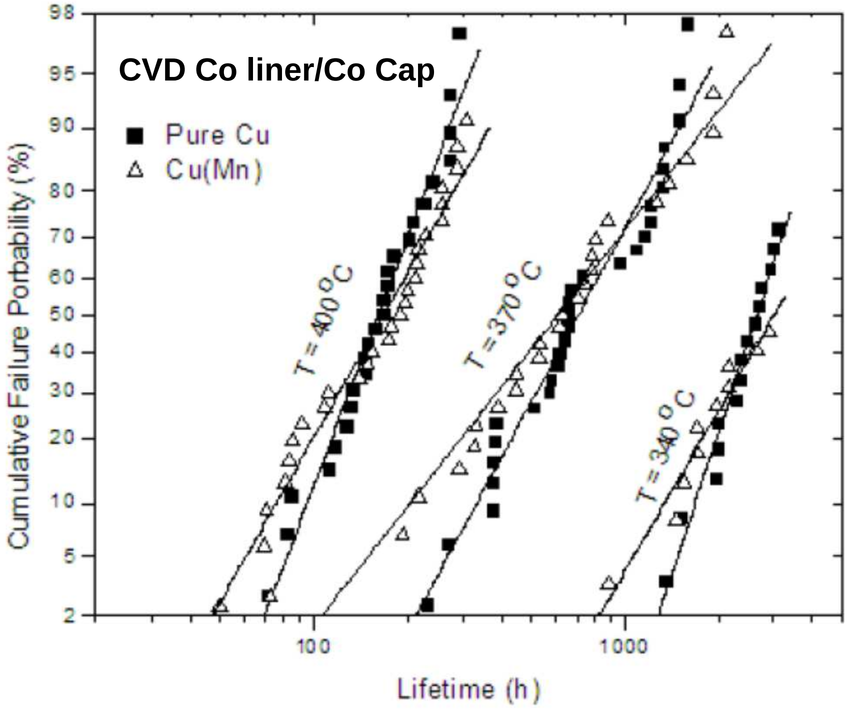


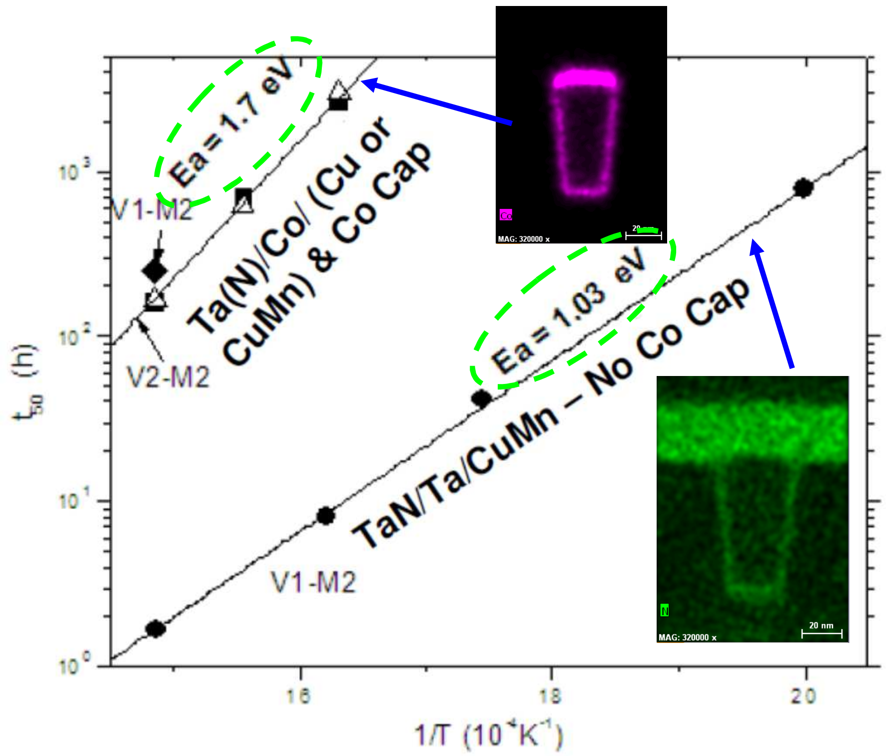
- Selective Co improves the adhesion interface between Cu and dielectric cap
- Complete wrap around structure with Co cap and Co liner provides optimum benefits

- TDDB failure probability on low k pSiCOH k 2.55
  - No degradation in selectivity, results comparable to dielectric only barrier film without Co

S. Nguyen et Al, ALD 2013 Conference Proceed.Vol. pp. 124-125 ., D. Priyadarshini, S. NGUYEN, IITC/AMC 2014 Conference Proceed. pp. 185-188

Activation Energy Results: Selective Co Cap/Co Liner





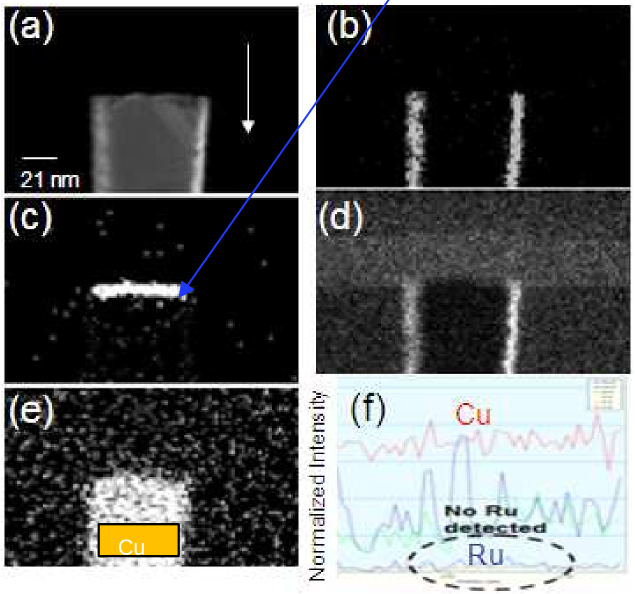
- **Line-depletion studies at 340C, 370C and 400C with selective Co cap/Co liner**
- **~100X median failure times with wrap around structure over TaN/Ta – Dielectric barrier scheme**

Wrap around Co cap/Co liner structure offers substantial EM improvement

ref: Simon, et al., International Reliability Physics Symposium, 3F.4, (2013)

Selective CVD of Ru Cap for Cu_low K interconnect

Ru3(CO)12 was used in Ru cap deposition at 200 C



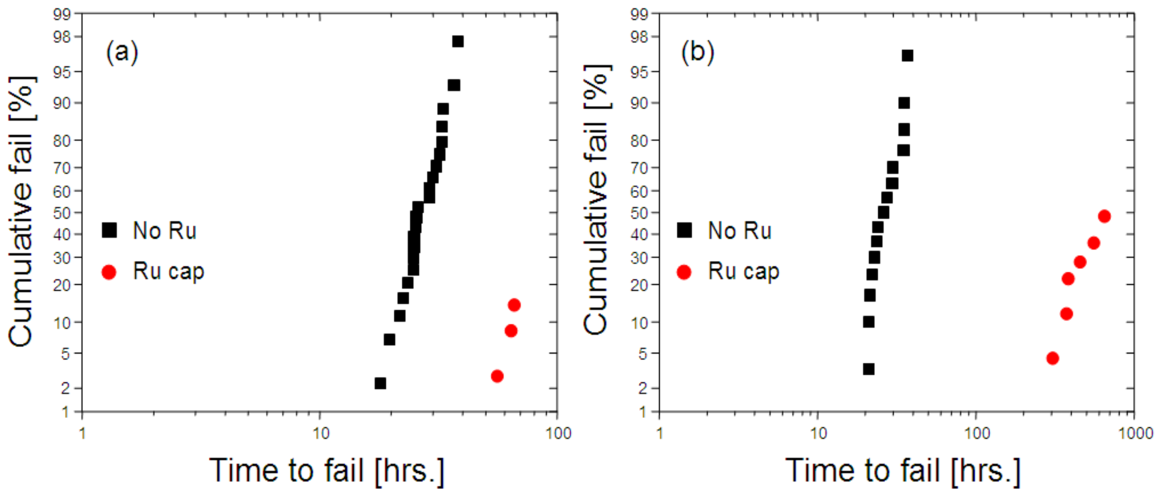


Table I. Deposited Ru thickness at various substrates (A).

Deposition time (s)	15	20	30	50	75
Temperature: 200°C					
Cu	6.3	—	14.0	—	—
Dielectric A	<1.0	—	<1.0	1.1	2.0
Dielectric B	<1.0	—	<1.0	<1.0	1.0
Temperature: 230°C					
Cu	9.3	—	20.4	—	—
Dielectric A	<1.0	1.4	2.6	6.3	10.3
Dielectric B	<1.0	<1.0	<1.0	2.6	6.5

70 nm Cu_ULK line and space Structure. Good EM improvement

C.-C. Yang et al ; Electrochemical and Solid-State Letters, 13 (5) D33-D35 2010.

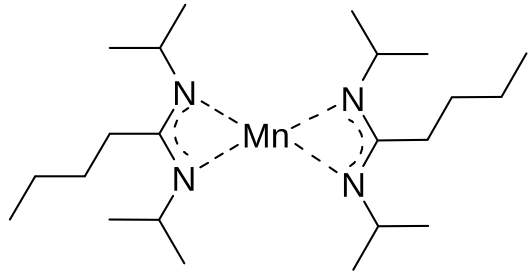
Chemical Vapor Deposition of Manganese

Precursors: Manganese and SAM

SAM=Self Assembly Monolayer (mostly Carbodisilane molecules) are used for surface treatment (prior to Mn deposition) to increase Mn deposition selectivity on Cu (vs p-SiCOH 2.2/2.4).

SAM1=*N,N*-Dimethyltrimethylsilylamine (C5H15NSi)

SAM2=Bis(dimethylamino)dimethylsilane (C6H18N2Si)

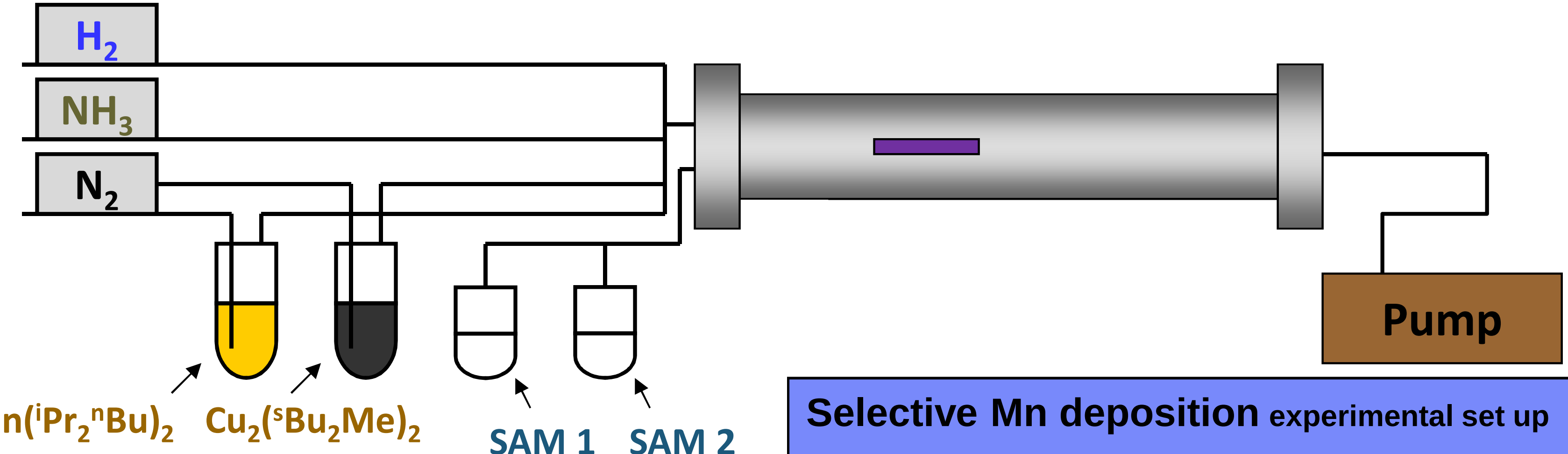


1)No Plasma Treatment step, No ULK damage

2) Precursor has No Oxygen→ No Liner oxidation

Name: bis(***N,N'-diisopropylpentylamidinato) manganese(II)***
Melting Point: ~60°C
Vapor Pressure: ~0.1 mbar at 90°C

CVD System Set up at Harvard for selective Mn deposition on Cu- Selectivity improved (30-40x higher, Cu/p-SiCOH :200-1000) with p-SiCOH/Cu pattern expose to SAM prior to deposition



Selective Mn deposition experimental set up (Nguyen…Gordon, Au.. Et al. , Proceed. ALD July 2015).

Capping Layer Application of CVD-Mn

Typical XPS analysis of Mn selective deposition with surface passivation using self-assembling monolayers (SAM)

Very High Mn selective is observed On Blanket Cu/SiO2-SiCOH film

Procedure

Reduction with Hydrogen

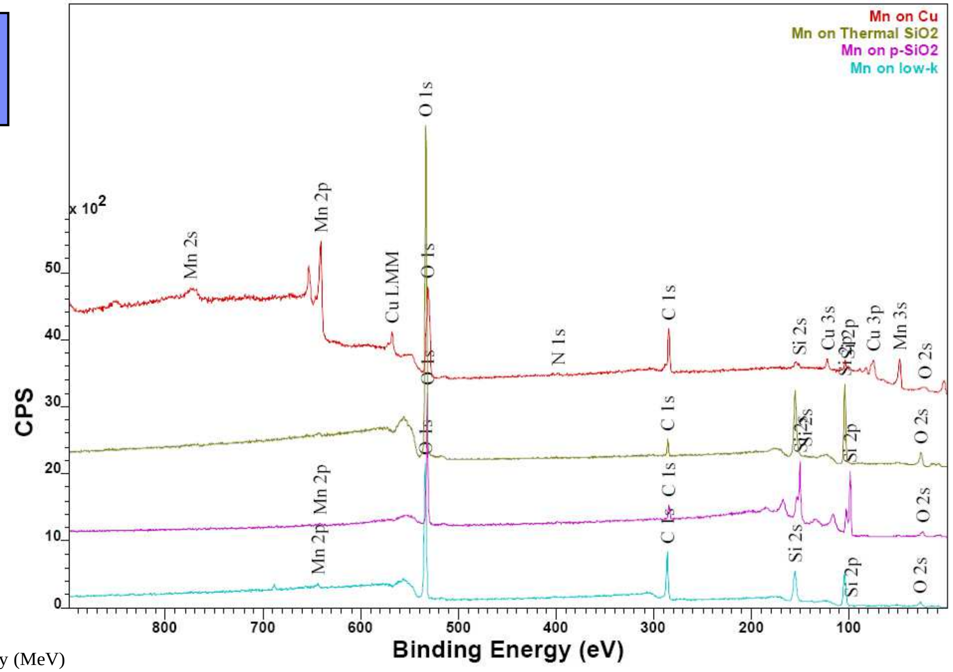
Surface Passivation with SAMs

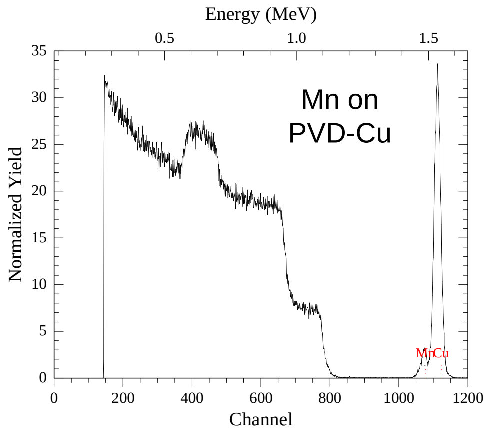
CVD-Mn Deposition

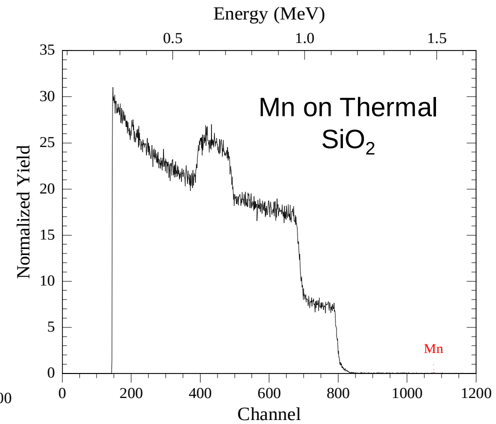
Process optimized for 90 nm pitch

Cu_pSiCOH k2.2

(Nguyen…, Gordon, Au et al. ALD 2015 ..)



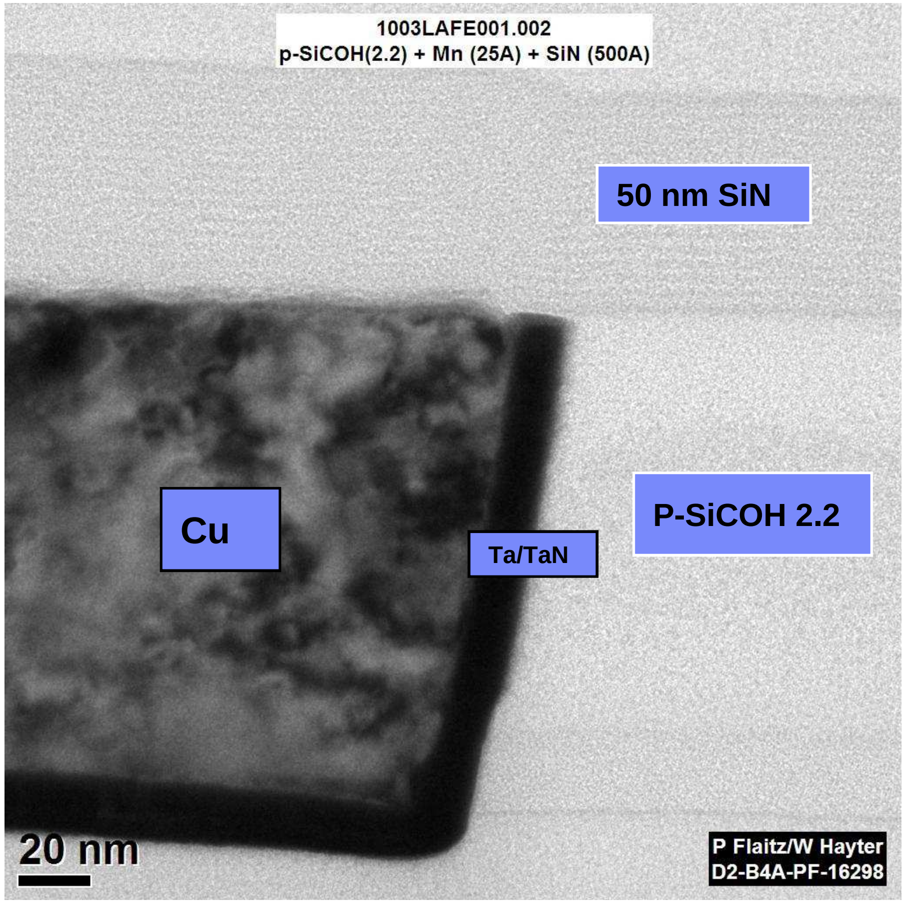


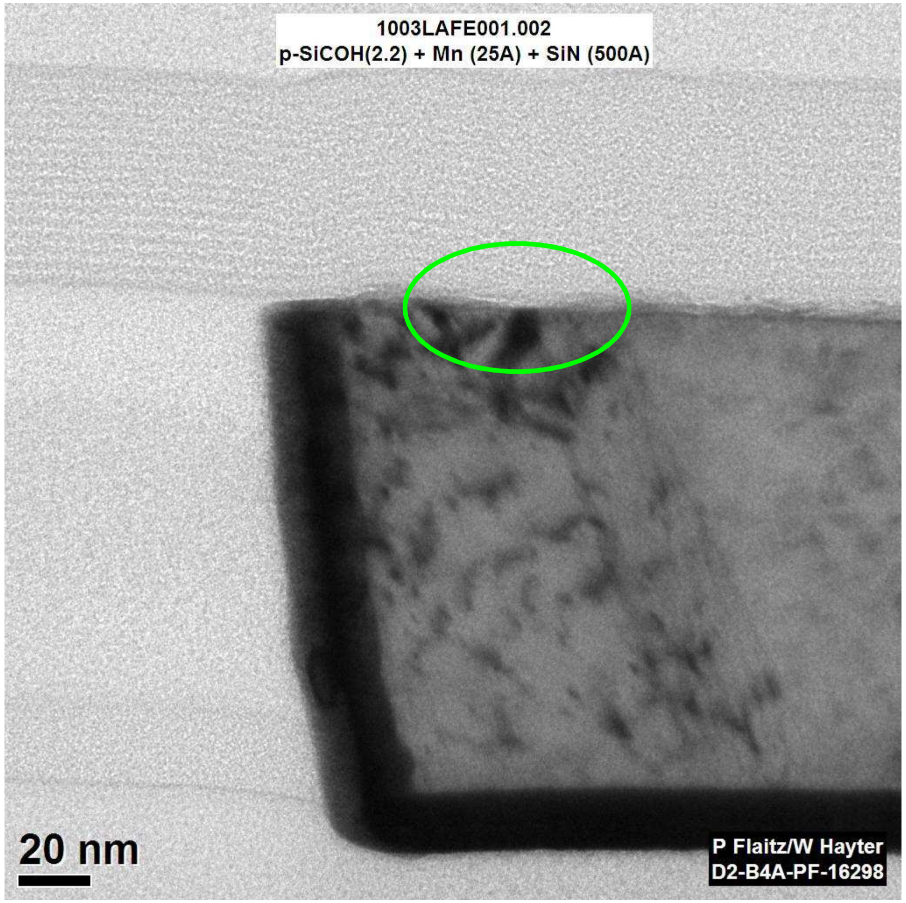


	Substrate	Mn Atoms	Selectivity
1	**PVD-Cu**	**1.45×10^{16}**	**--**
2	**Thermal Oxide**	**$<5 \times 10^{13}$**	**>290:1**
3	**p-SiO_2**	**$<5 \times 10^{13}$**	**>290:1**
4	**Low-k pSiCOH k 2.2-2.7**	**$\sim 7 \times 10^{13}$**	**207:1**

- Selectivity over 200:1 can be achieved

TEM of selective Mn deposition on 90nm pitch M1 Cu-p-SiCOH 2.2 pattern structure



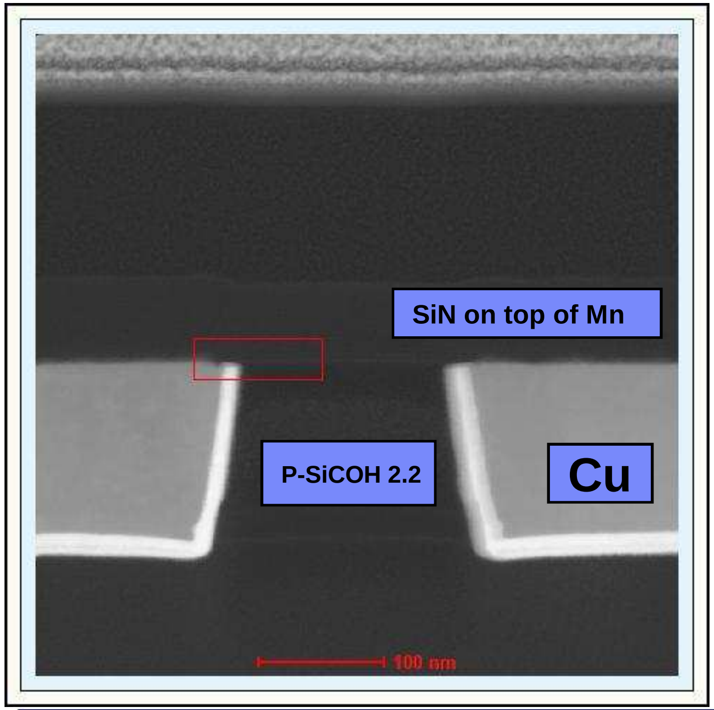


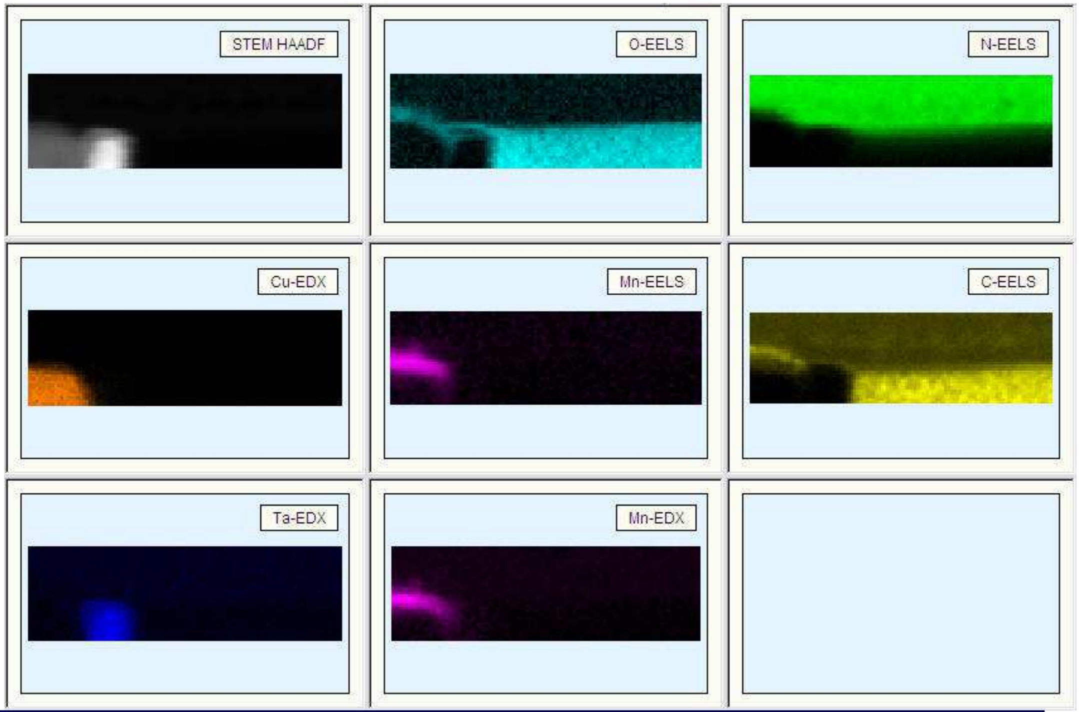
Detailed views of the surface of two of the structures near the edge of the lines. The Mn deposition is clearly present on top of Cu and none p-SiCOH 2,2 , though apparently thin Mn in the indicated location (oval).

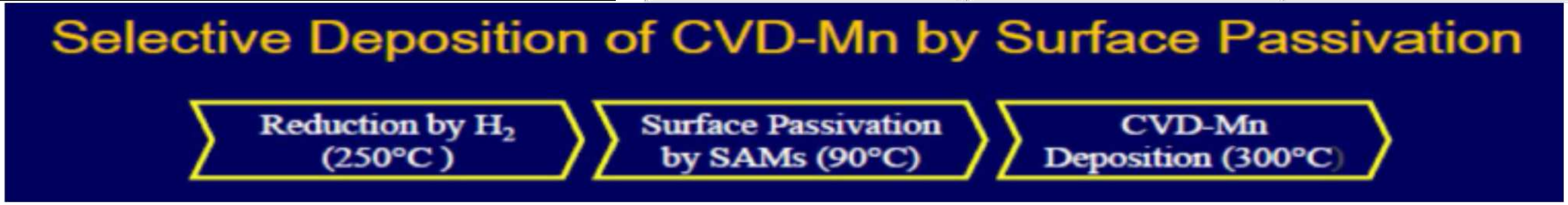
The expected Mn thickness is 2.5 nm, the TEM measured Mn thickness is ~3 nm

(Nguyen… Grodon, Au et al. , ALD 2015)

TEM/EDX/EELS analyses of Selective Mn deposition on 32 nm M1 Cu-p-SiCOH 2.2 pattern structure





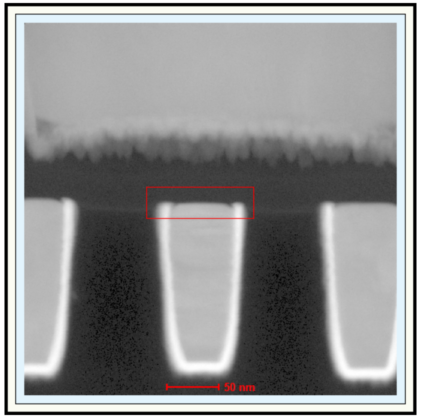


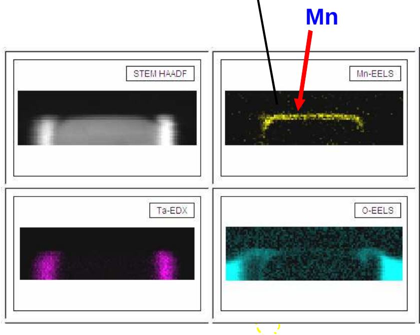
Similar EDX/EELS maps were obtained at the edge of a line, over the low-k surface (red rectangle in STEM image at left). Maps at right show no indication of Mn over the ULK or over the Ta liner, only over the Cu surface. **EXCELLENT CVD Mn selectivity on Cu confirmed.**

(Nguyen…, Gordon, Au et al., ALD 2015 Proceeding)

Selective Mn will form complete Wrap around with SFB Mn Liner

SFB Mn metal Cap

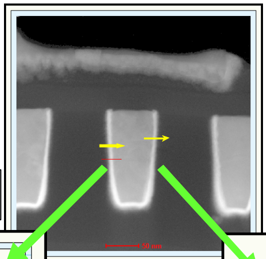




CuMn6at% Seed

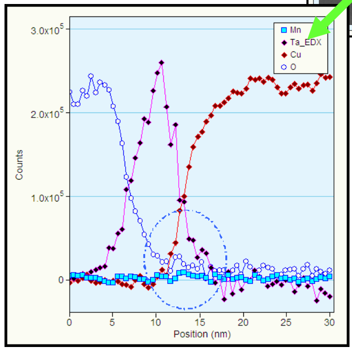
Cu Mn IBM Scheme (Nogami). CVD Mn/MnNx will eliminate the need for CuMn (2-10 % Mn) seed in Self Forming Barrier (SFB) scheme that impact resistance greatly. CVD MnSiOx/MnSiCOH, and MnNx also show promising barrier potential… that minimize the negative impact of litho/etch profile and dimension control variability. With the self-limiting reaction, the SFB enable 1-2 nm liner thickness. In SFB approach, Mn concentration in Cu can be high (2-10% wt) and negatively impact (increase) Cu resistivity. NEED better Mn SFB source

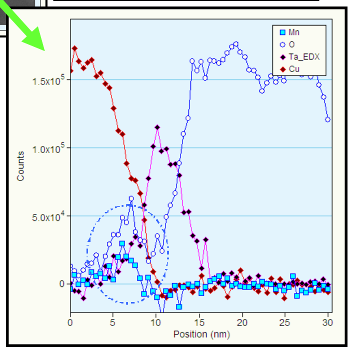
EELS shows Mn accumulation across entire Cu/NBLOK interface, and curving over into liner interface



The left side has no indication of Mn at the Cu/liner interface.

The right side has indication of Mn and O at the same time.



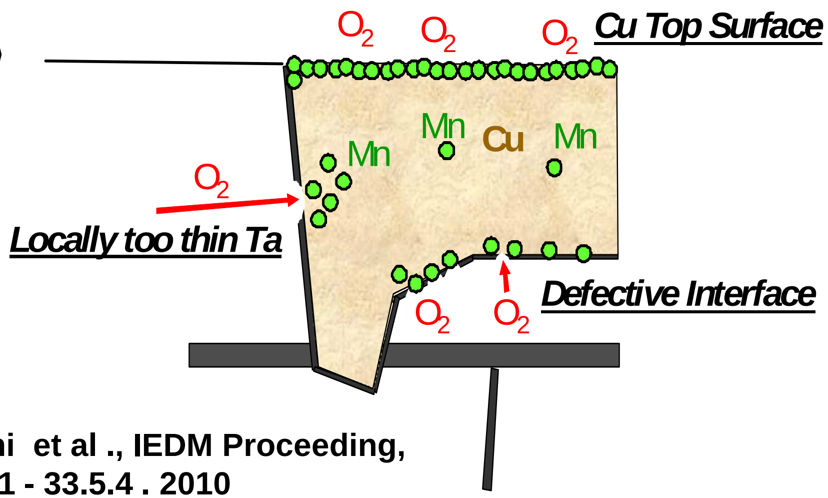


PVD asymmetry created a thinner TaN on the right side where Mn accummulated to trap oxygen which invaded from low-k to copper.

Manganese Scabbing Model

Blood platelet reacts on oxygen in the air to form scab on our skin, when injured.

Mn reacts on oxygen at the surface and at defects to form MnO.



Nogami et al ., IEDM Proceeding, p.33.5.1 - 33.5.4 . 2010

Mn makes perfectly coated Cu lines → Excellent EM performance

Feasibility Study : **Selective Mn** deposition on 90 nm pitch **Metal 1 chip**

200A (20nm) Mn deposited at 300 C with ½ hour ramp up and down-Chip passivated with 150A PECVD SiNx

The Mn deposition selectivity of un-passivated on p-SiCOH (2.2/2.4) over Cu are 4:1 and 25:1 respectively

The Mn deposition selectively on Silicon-based SAM on p-SiCOH (2.2/2.4) over Cu are higher (200-1000 range)

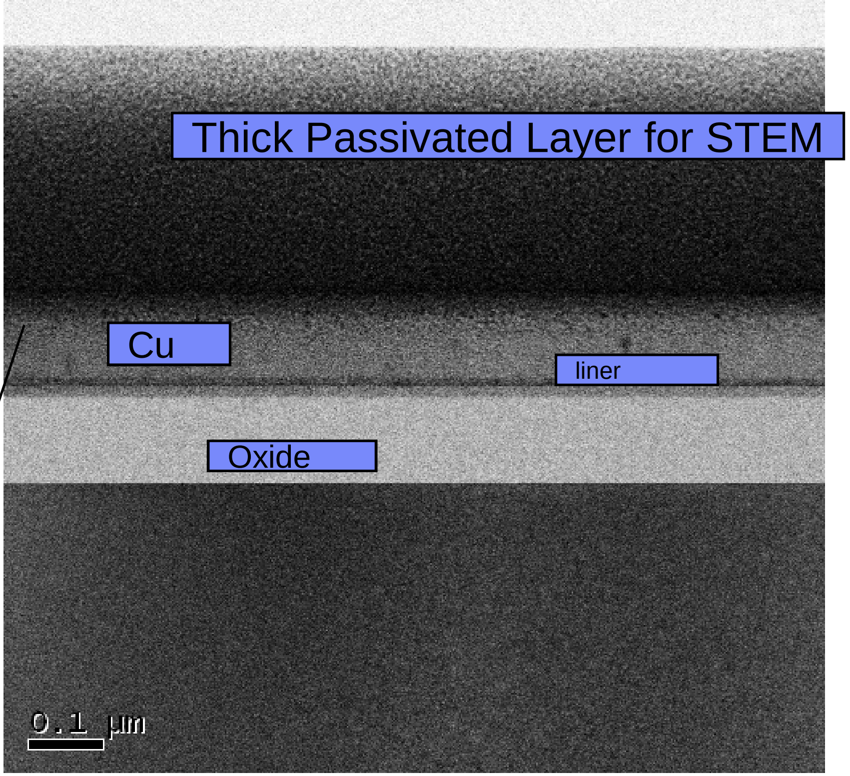
Low Leakage but ~20% increase in Cu resistance for Thick 20 nm Mn

Device	Initial Resistance (ohms)	Initial Leakage (amps)	Resistance after Heating (ohms)	Leakage after Heating (amps)
REMONCD	459,900	4.43E-09	568000	1.00E-06
REMONAB	482,700	5.38E-09	619950	3.54E-09
	Leakage @ 5 volts			
	Resistance measured @ 10 microamps			

Selective Mn deposition on Cu reduce the Cu line to line leakage

Cu resistance increase due to Mn diffusion into Cu.

Need additional optimization



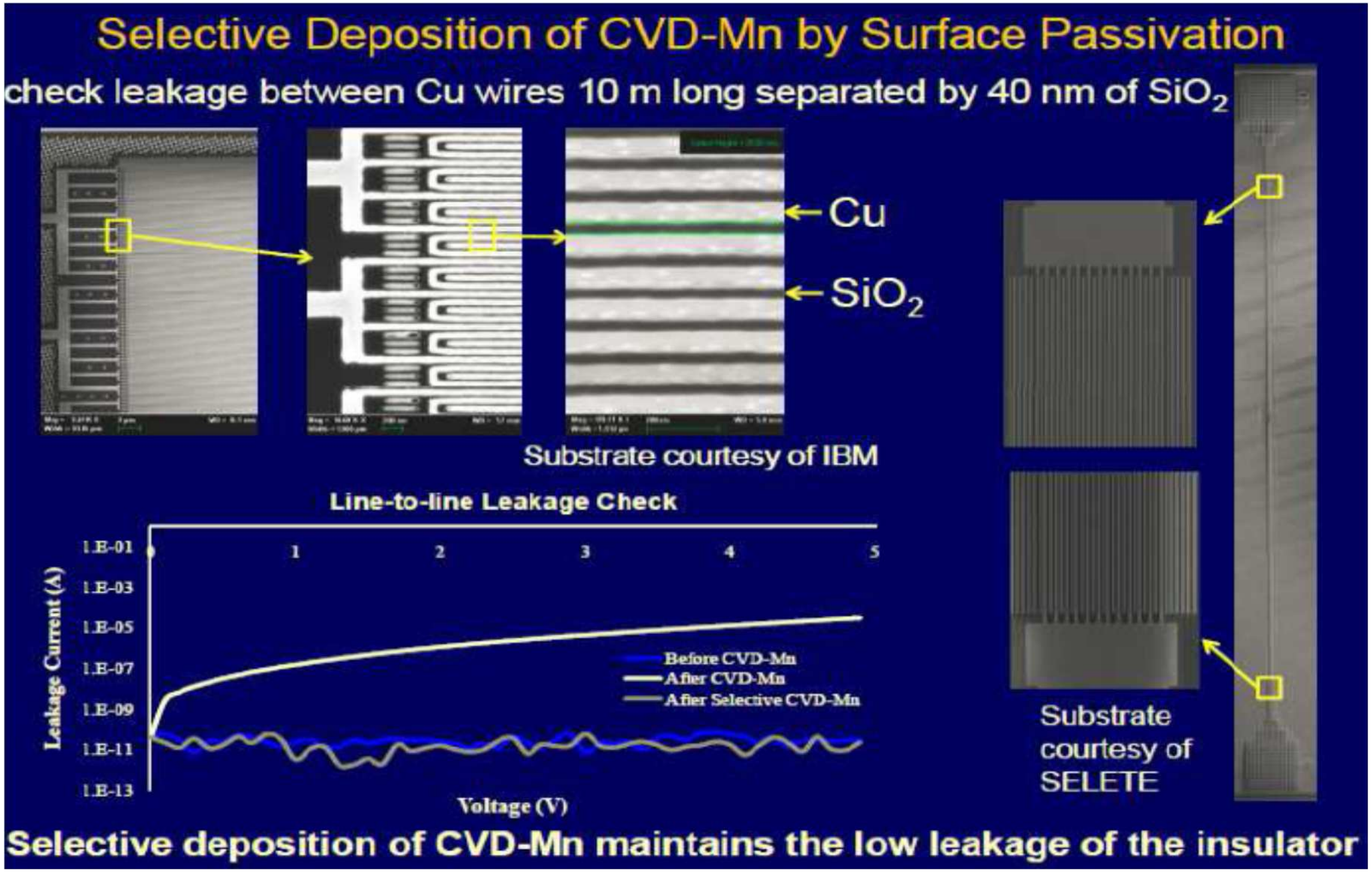
Mn Diffuse into Cu and increase resistance

Need to reduce the amount of Mn deposited

Nguyen…Gordon, Au et al. , ALD 2015 proceeding)

CVD –Mn form MnSiOx and maintain low leakage of insulator MnSiCxOy or MnSiCxNyOx may have same performance

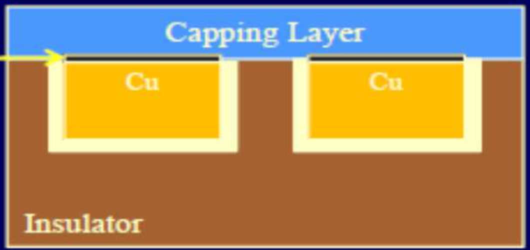
(R. Gordon et al. , Vapor Deposition of Materials for Microelectronic Seminar, 2012)



Self-aligned Mn/MnSixOyNz potentially enable sub-5 nm cap thickness and wrap around SFB Mn Liner/Mn Cap for sub-7 nm BEOL Cu-Low k

Increase lifetime before failure by electromigration

Self-aligned barrier/adhesion layer



- Selectively deposit manganese on Cu wires to form a CuMn alloy
- Deposit capping insulator layer (Si_3N_4 or SiCN) on top
- Anneal to allow manganese to diffuse to the Cu/capping layer interface
- Manganese enhances adhesion at the interface and forms a self-aligned $MnSi_xO_yN_z$ diffusion barrier

Y. Au, Y. Lin, H. Kim, E. Beh, Y. Liu and R. G. Gordon, "Selective Chemical Vapor Deposition of Manganese Self-Aligned Capping Layer for Cu Interconnections", *J. Electrochem. Soc.*, **157** (6) D341-D345 (2010)

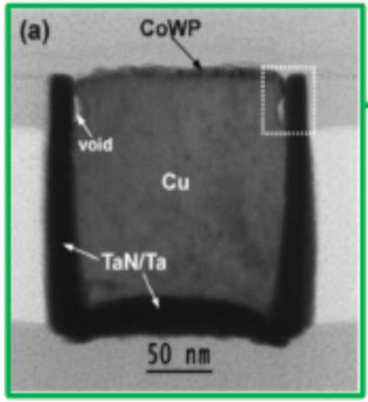
Summary

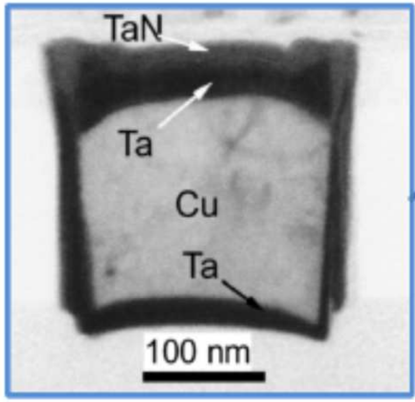
- **Advanced ultra-thin metal caps are required to enhance electro-migration reliability in sub-20nm Cu interconnects.**
- **CVD/ALD Selective metal deposition provides one of the best approaches to form selective metal cap on Cu for ultrathin cap with film's reliability performance.**
- **Various selective CVD Cobalt, Ruthenium, Manganese caps were evaluated: Selective Co cap/Co liner (wrap around structure) on Cu shows the best EM improvement without any TDDB degradation in sub-20 nm Cu interconnect.**
- **Selective CVD Co is currently implement in industry Fabs.**

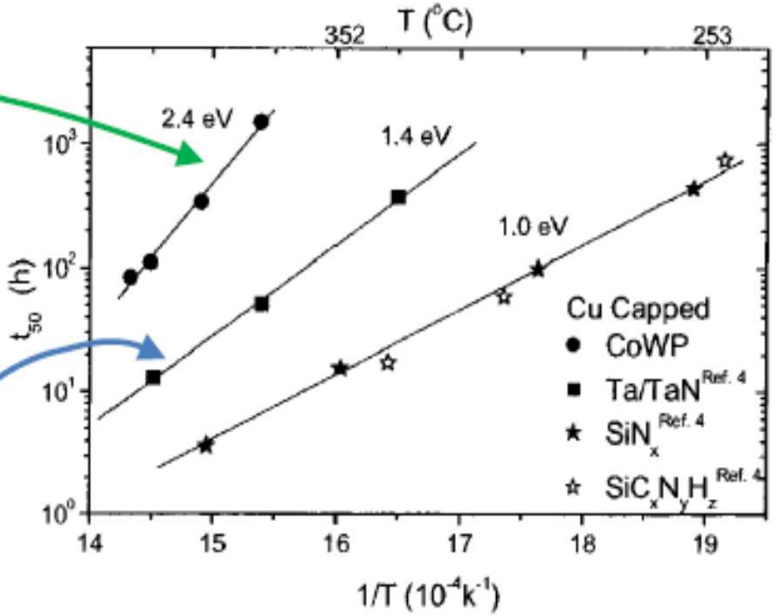
Back Up Foils (Only show if needed)

Metal capping prevents fast Cu diffusion path at top surface

- Significant improvement compared to dielectric caps (SiN or SiCHN)





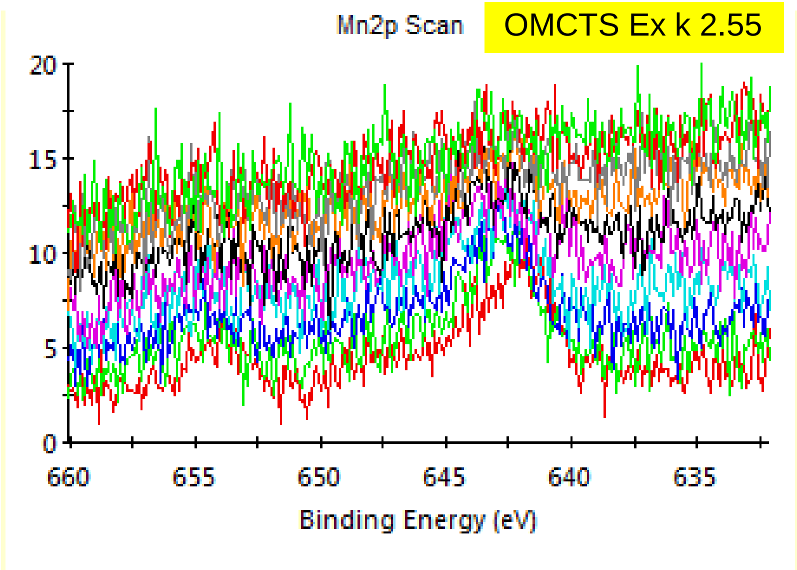


C. K. Hu, *et al.*[1-3]

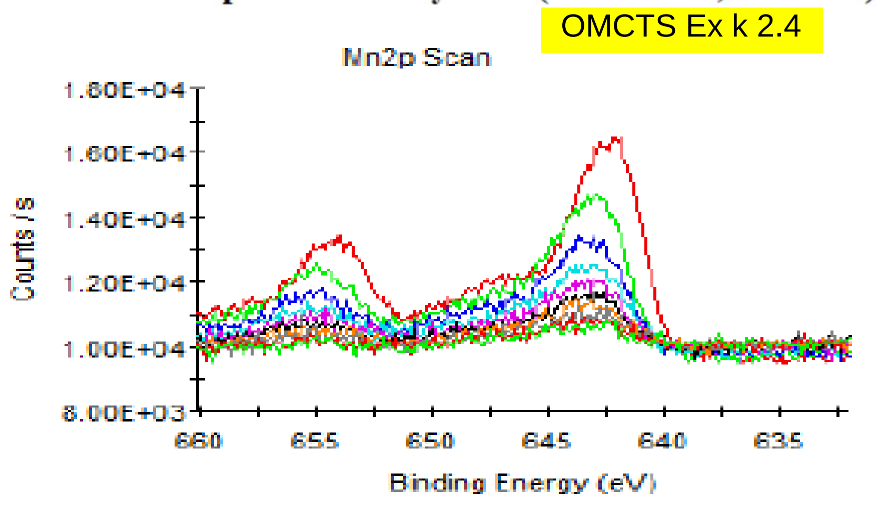
[1]C.-K. Hu, ***et al.***, Appl. Phys. Lett. 81, 1782, 2002; [2]C.-K. Hu, ***et al.***, Appl. Phys. Lett. 83, 869, 2003; [3]C.-K. Hu, ***et al.***, Appl. Phys. Lett. 84, 4986, 2004;

Mn Diffusion in pSiCOH: OMCTS Ex k 2.55, 2.4

Depth of penetration of the Mn by XPS (1nm/level) :



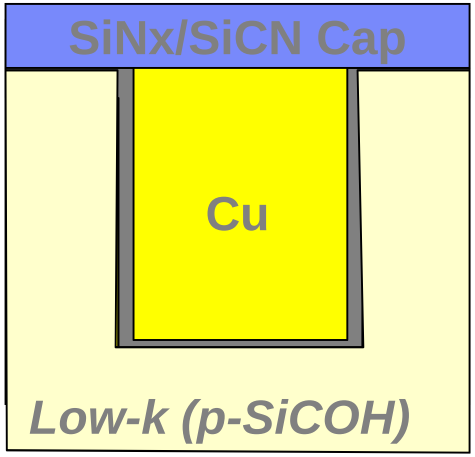
Mn penetration by XPS (~1nm/level, 10 levels)



5min UV

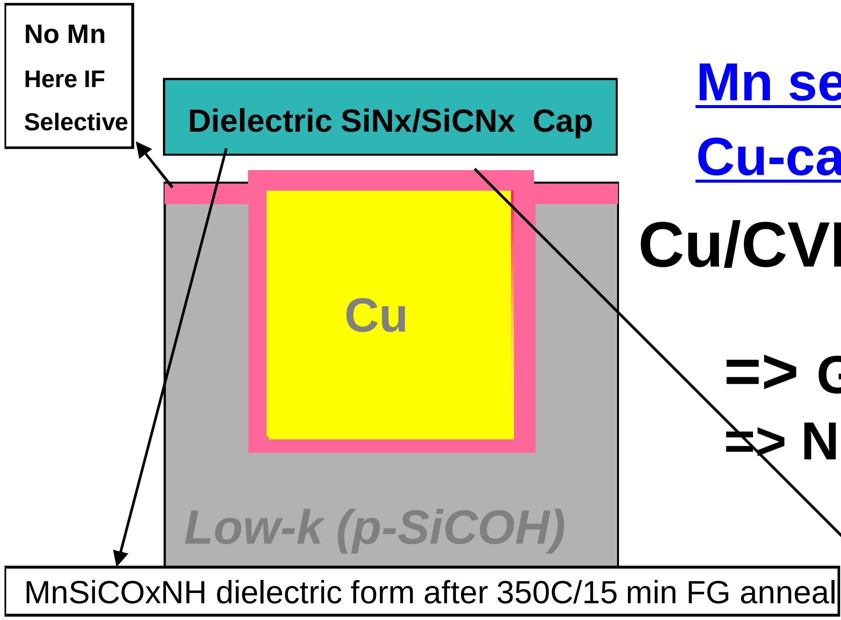
- Mn amidinate precursor used for Mn deposition on OMCTS Ex film → <u>no significant penetration of Mn detected in this ILD material</u>
  - Pores in OMCTS Ex smaller than amidinate precursor and prevents diffusion of Mn in low k
  - Other types of pSiCOH ULK 2.4 showed significant Mn penetration
  - UV curing the surface prior to Mn deposition makes the surface hydrophilic – some Mn detected in UV cured sample

CVD thin Mn form MnOx (remove O in Cu surface)→ enhance Cu-dielectric adhesion and EM



Issues of current dielectric (SiCN) capping layer

- Sub 30 nm Cu and SiCN cap interfaces
→ Low electromigration resistance
- Need non plasma CuOx removal
- → No plasma damage on p-SiCOH



Mn self-aligned capping layer- Our focus on Cu-cap surface and MnOx-pSiCOH ILD

Cu/CVD Mn(sel. prefer) /Dielectric+ anneal

=> Good Cu adhesion to insulator cap
=> No dielectric-Cu interfaces in this case.

Dielectric-Mn/MnOx-Cu interface formation
-→ Improve EM

- Nguyen.. Gordon, Au, et al ALD 2015 Proceed.

Typical resistance and leakage changes in 90 nm pitch Cu-pSiCOH k2.2 structures (~90 nm pitch) after various process/treatment steps of selective and evaporated (NON-SELECTIVE) Mn deposition

Sample No /(Mn thickness, nm/process)	% (Pre-Post) 300C anneal Serp Resistance change	Comment	% (Pre-Post) 300C anneal Leakage change	Comment
1 (0.5nm sel. CVD Mn)	(-1%)	Good	1.5 %	Good, No change
4 (1nm sel. CVD Mn)	(-2%)	OK	2%	OK, no real change
5,7 (2.5nm sel. CVD Mn)	~1-3%	Small change	2-3.5%	minimal increase
A (20nm sel. CVD Mn)~10%	20%	Large increase	3.2%	Small increase
1A(0nm/H2/SAM/Cap)	1%	No change	(-1 to 2%)	No change
2B (0 nm, H2/Cap)	(-1.5%)	No change	>(-2%)	No change
3A(0 nm, cap)	(-2.5%)	H2O outgas	~(-3%)	H2O outgas
NON-Selective (YKT) Evaporated Mn (0.5,1,2,3 nm)- Whole wafers (patterned)		Non Selective Mnt	Almost all device has small leakage,	Non Selective Mn CVD cause small leakage. Required annealing

Selective Mn CVD processing steps:

1) H2= H2 reduction 250C for 1hr;

2) SAM= Self Assembly Monolayer TREATMENT for 90c, 30 min (SAM1=*N,N*-Dimethyltrimethylsilylamine (C5H15NSi), SAM2=Bis(dimethylamino)dimethylsilane (C6H18N2Si))

3) Selective deposition of Mn (0, 0.5, 1, 2.5 and ~20 nm) with bis(*N,N'-diisopropylpentylamindinato) manganese(II)+ Hydrogen*

4) Cap = Capping layer (~50 nm PECVD SiNx) deposited at 300 C

SELECTIVE Mn (0.5-2.5 nm) cap deposition cause minimal Cu resistance and leakage change in 90nm pitch Cu-pSiCOH k 2.2