

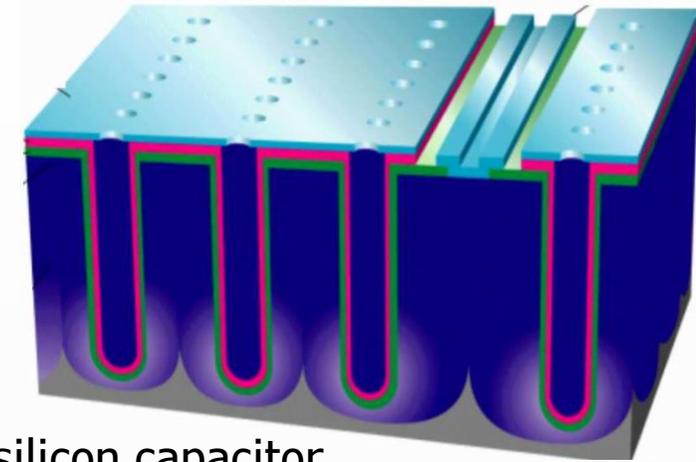
PillarHall LHAR Silicon Chips by Chipmetrics

Author: Mikko Utriainen, Chipmetrics
Spatial ALD 2022 Eindhoven 09.06.2022



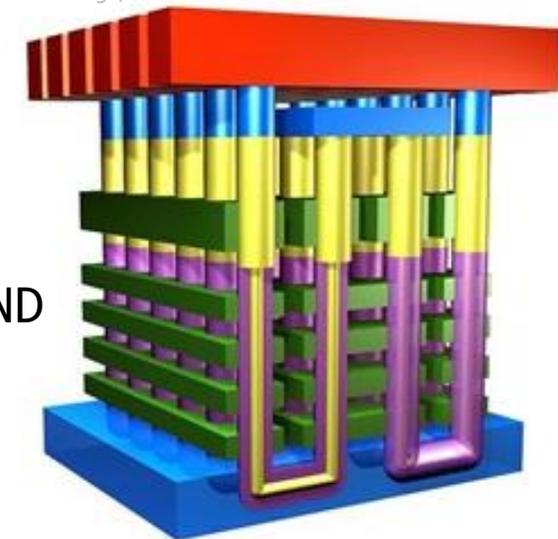
3D is a megatrend

- To improve performance and energy efficiency of microdevices
- Applications e.g.
 - **Semiconductors:** 3D-NAND, DRAM, TSVs, FinFET, GAAFET, etc ..
 - **Photonics, MEMS, microfluidics, etc**



3D silicon capacitor

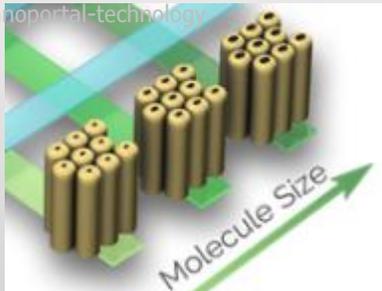
<https://anysilicon.com/overview-and-types-of-capacitors-in-asic-design/>



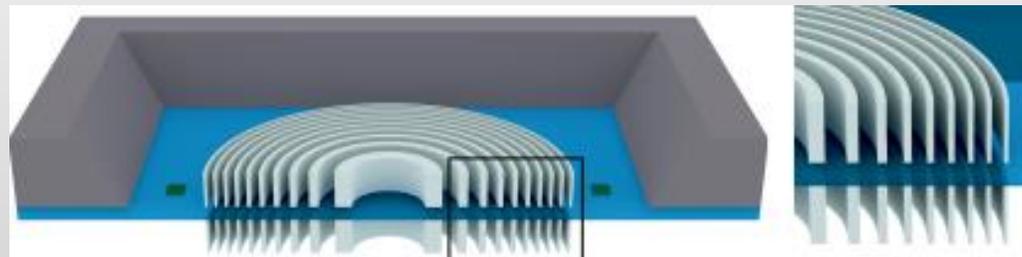
3D NAND

<https://www.newelectronics.co.uk/electronics-technology/3d-structures-to-dominate-the-flash-memory-market/155486/>

Nanoprecision Medical Ltd
<https://www.nanoprecisionmedical.com/technology/nanoportal-technology>



Microfluidics

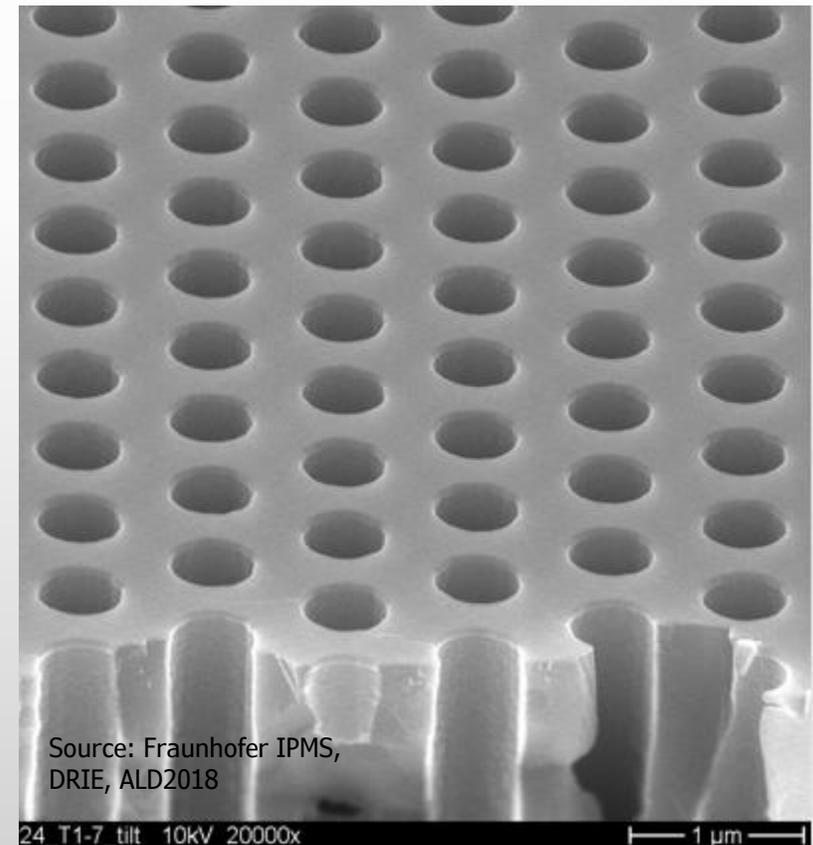
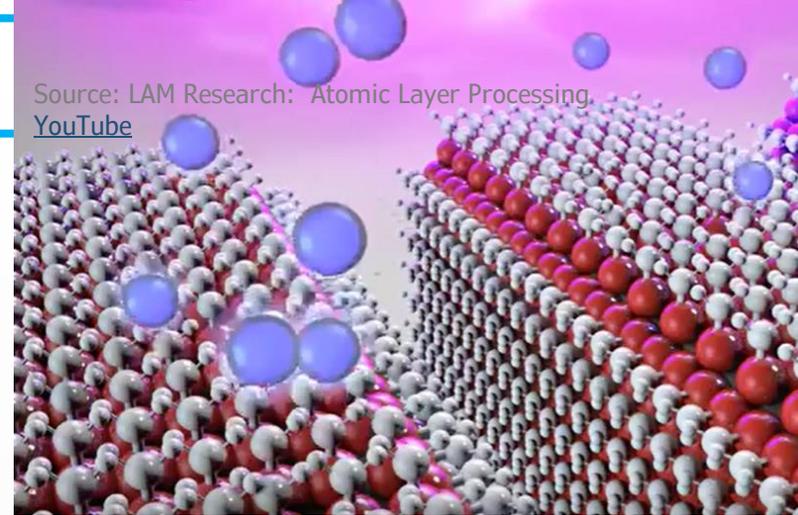


Mohacsi et al Optics Express (2015) <https://doi.org/10.1364/OE.23.000776>

Photonics

Atomic Layer Deposition (ALD) is a Technology for Conformal Thin Films

- For high quality manufacturing of 3D microelectronics and advanced materials
- Boosting 3D vertical scaling trend
 - 3D-NAND, 3D-DRAM, TSVs, FinFET, GAAFET, PCRAM, FeRAM, etc ..



3D THIN FILM METROLOGY IS A PROBLEM



Needs cross-sectioning

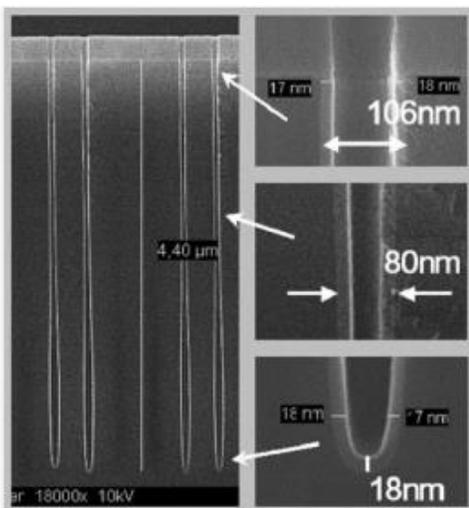
- Destructive. Special tools and users.
- Slow. Expensive. Slow.

3D substrates not accessible

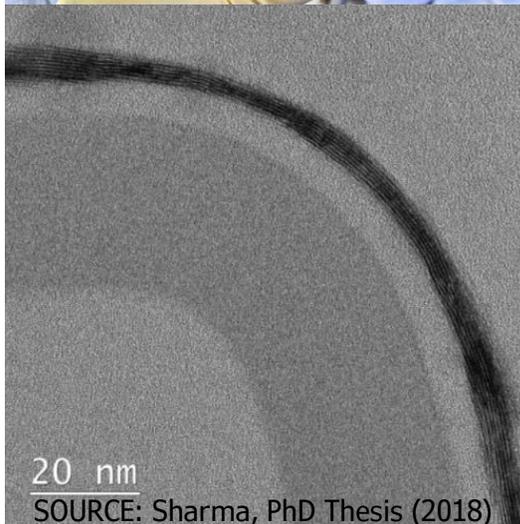
- Proprietary. Inaccurate quantification.
- Expensive. Lack of standards.

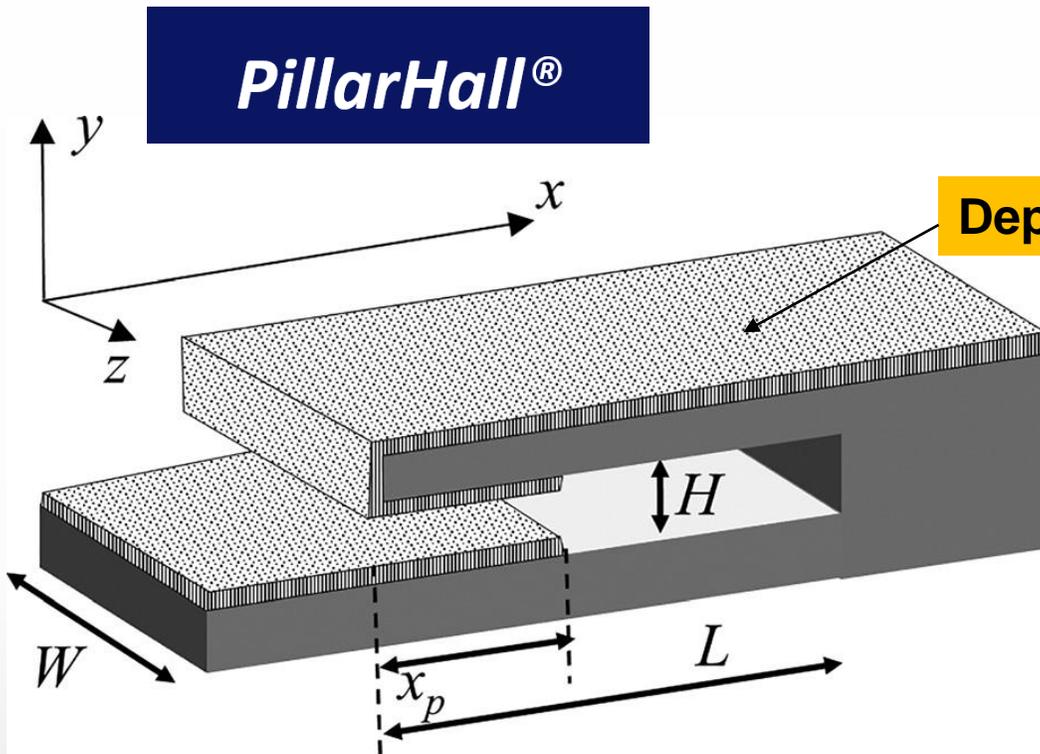
Huge parameter space in ALD

- Importance of speed



Gutsche, Future Fab Intl. Issue 14
George, plenary talk, AVS-ALD 2013

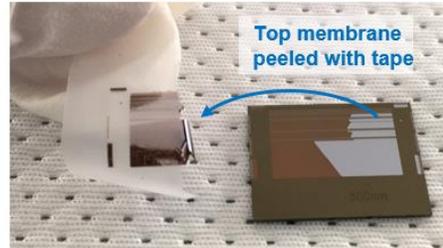




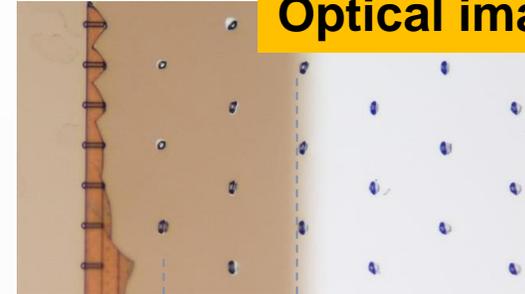
PillarHall®

Deposit thin film

Analyses after removal of top membrane
PillarHall® line scans: route to understanding and optimising process fundamentals



Optical imaging



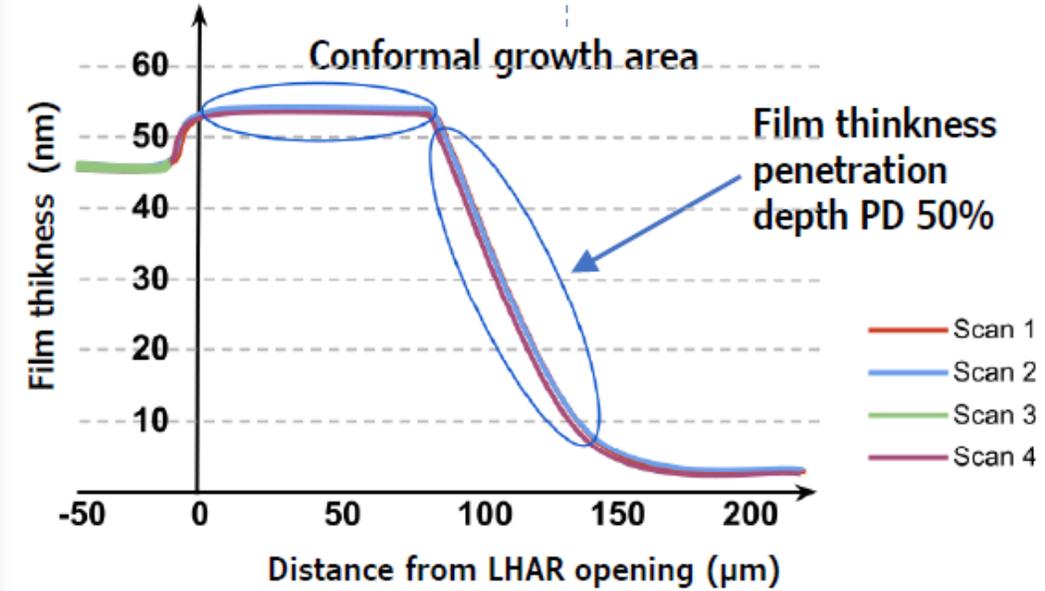
Specroscopy line-scans

ASPECT RATIO

- 10000:1; 2000:1; 1000:1; 200:1; 100:1;
- 40:1; 20:1; 10:1; 2:1

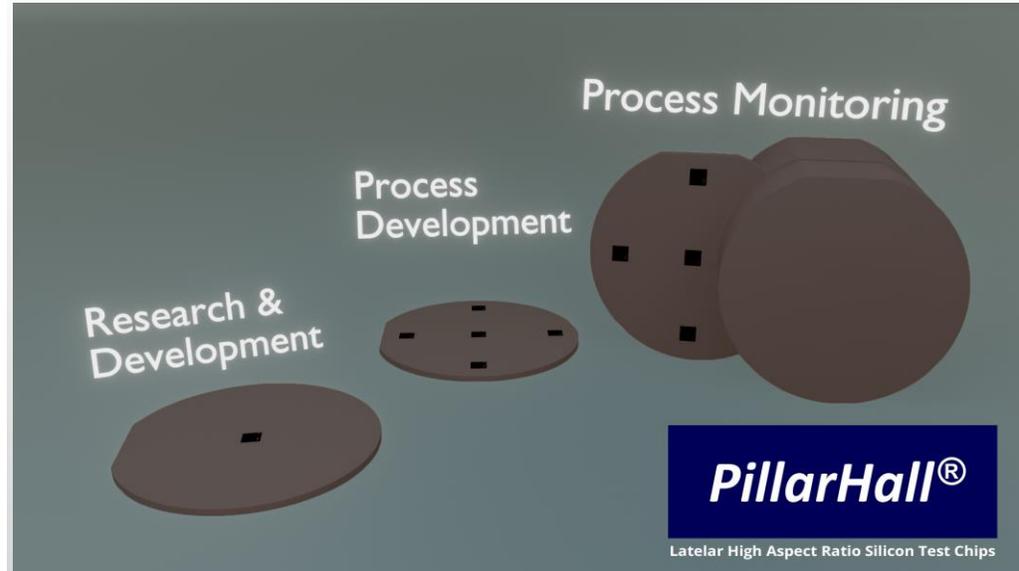
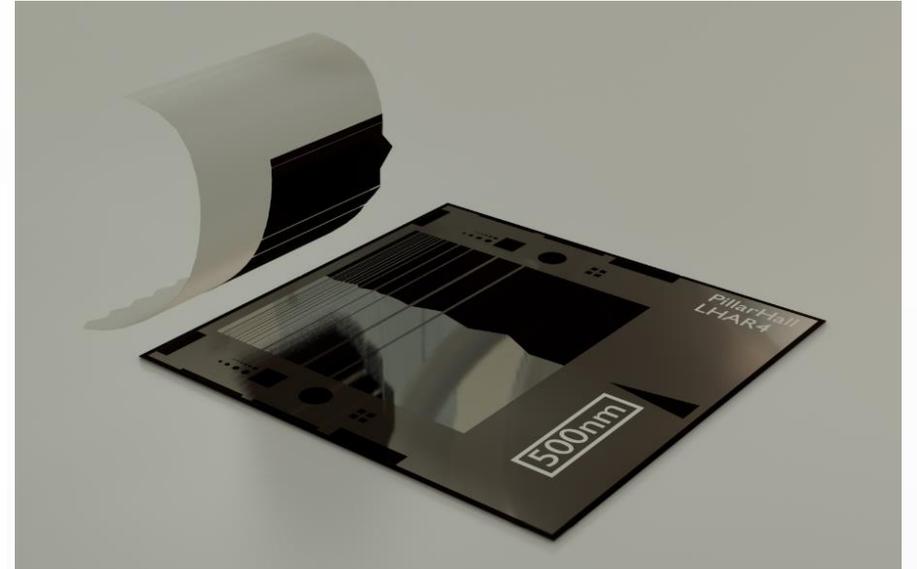
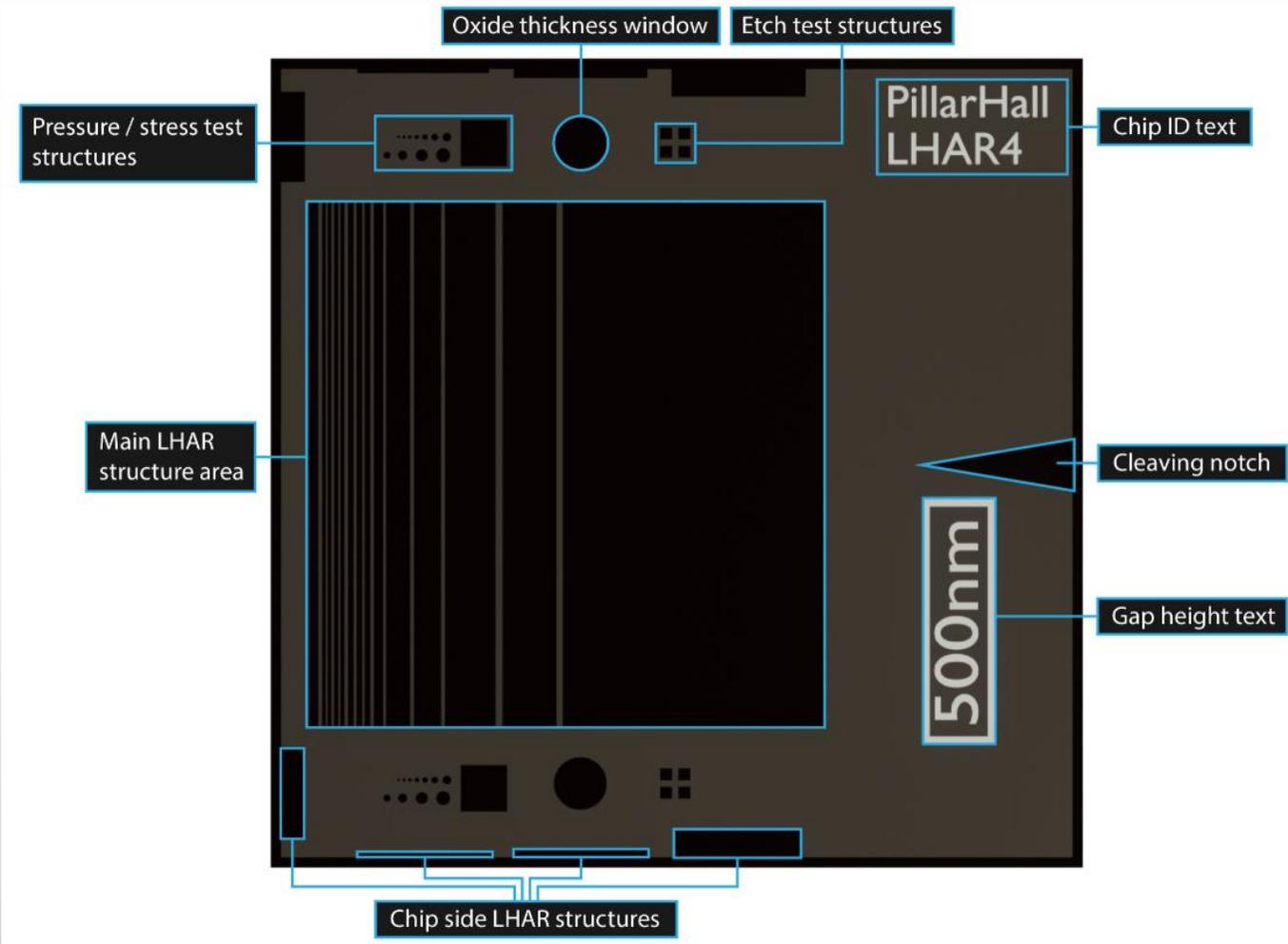
Ylilammi et al. Journal of Applied Physics 123, 205301 (2018)

Measure: film thickness as a function of film penetration depth



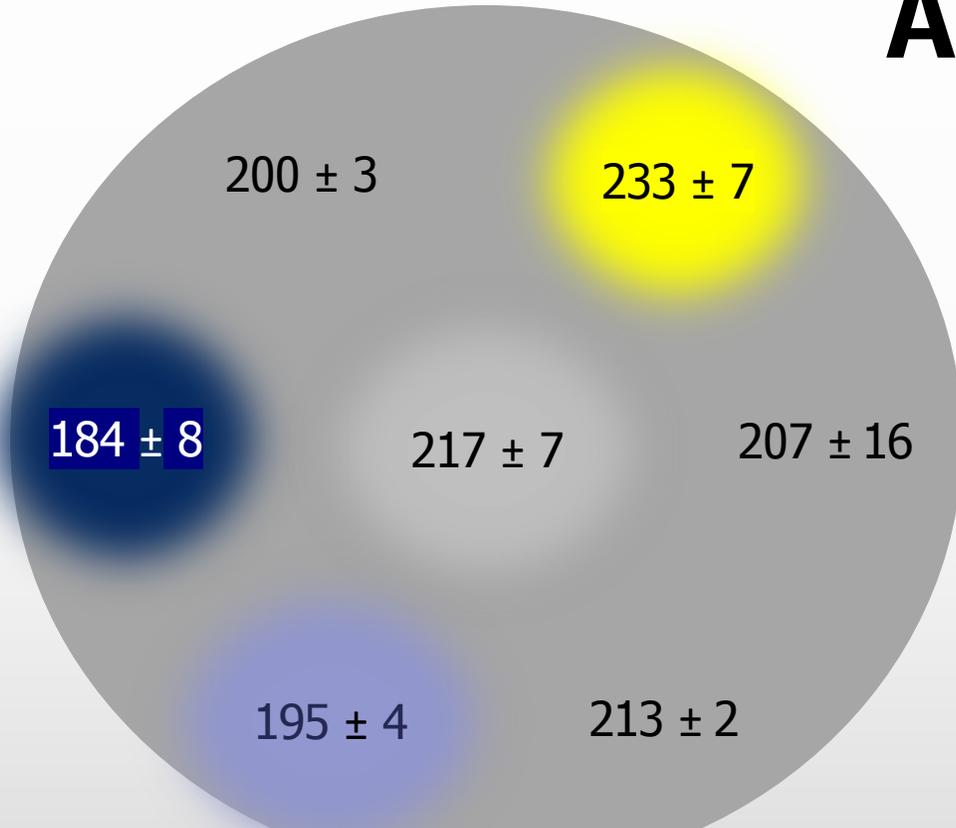
PillarHall®

LHAR4 Test Chip



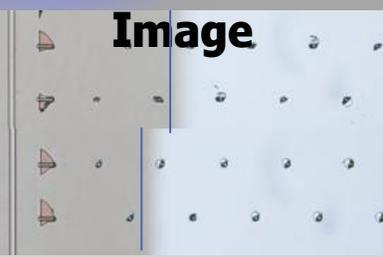
VTT process, 500 cycles

150 mm wafer.



max 233 ± 7

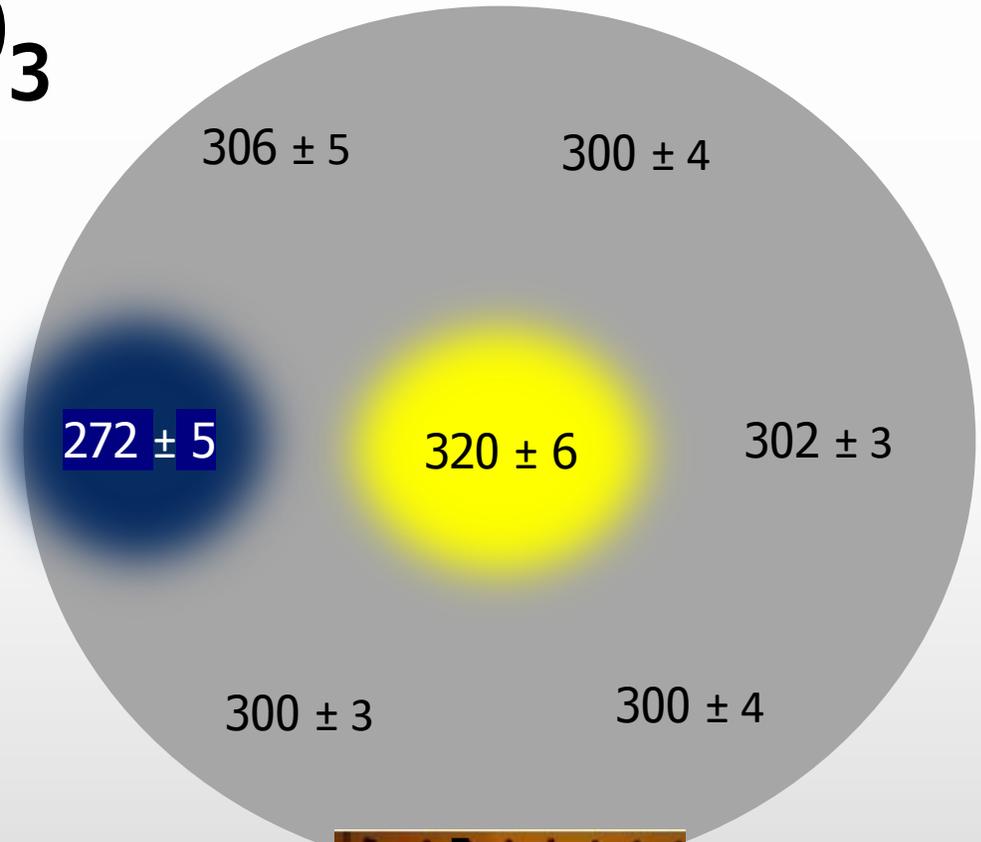
min 184 ± 8



$\Delta_{\min-\max} = 21\%$

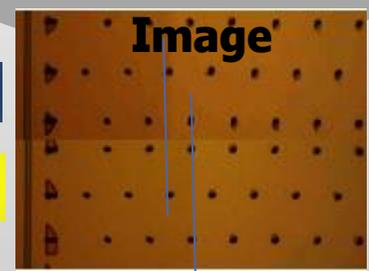
UEF process, 125 cycles

200 mm wafer.



min 272 ± 5

max 320 ± 6



$\Delta_{\min-\max} = 15\%$

High Aspect Ratio (HAR) geometry correlation

How to compare PillarHall data to the HAR target?

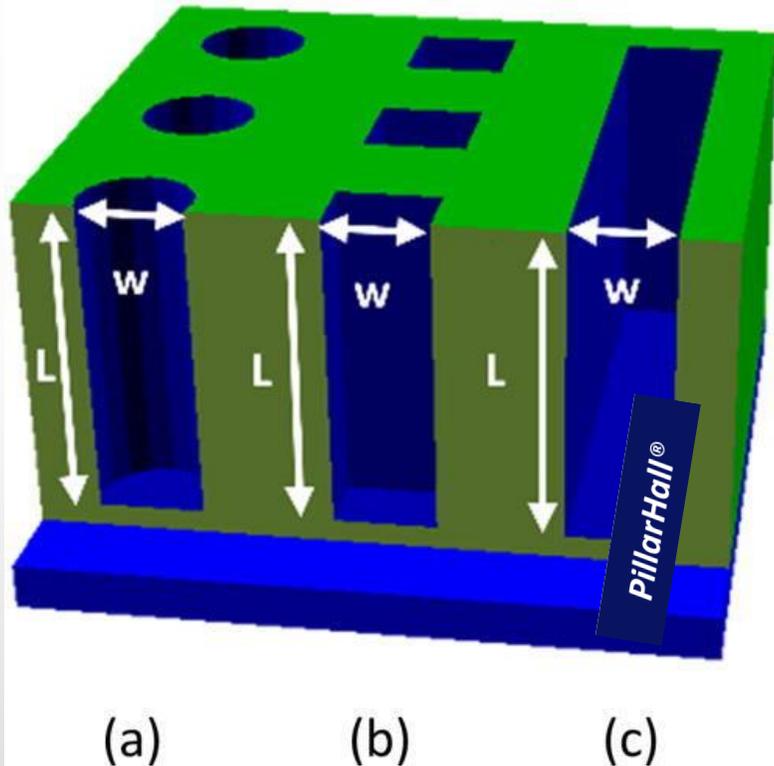


Fig.1. High Aspect Ratio geometries:
 (a) Cylindrical hole, (b) a square hole, (c)
 trench, with width w , and depth L

$$\text{Equation: } a = \frac{Lp}{4A}$$

with

a being aspect ratio,

L (m) being the depth of the cavity,

p (m) being its perimeter, and

A (m²) being the cross-sectional area.

For trenches, the equation reduces to

$$a=L/2w,$$

while for holes it reduces to

$$a=L/w.$$

BREAKING:
HAR comparison
calculator tool
available by
Chipmetrics

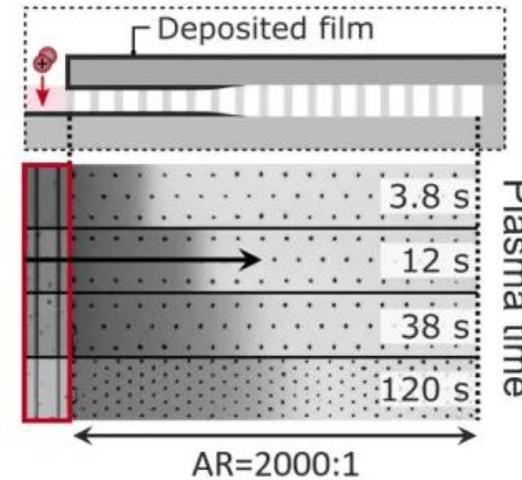
PillarHall in Research

- **Conformality in thermal & plasma ALD**
 - Understanding conformality
 - Extracting sticking coefficients
 - Extracting plasma recombination probabilities
- **Conformality in CVD**
 - Surface-inhibiting growth
 - Metal CVD conformality
- **Properties of the film on the trench wall**
 - Compositional dopant mapping
 - Wet etch rate
- **Film stress in the microscale**

And more..

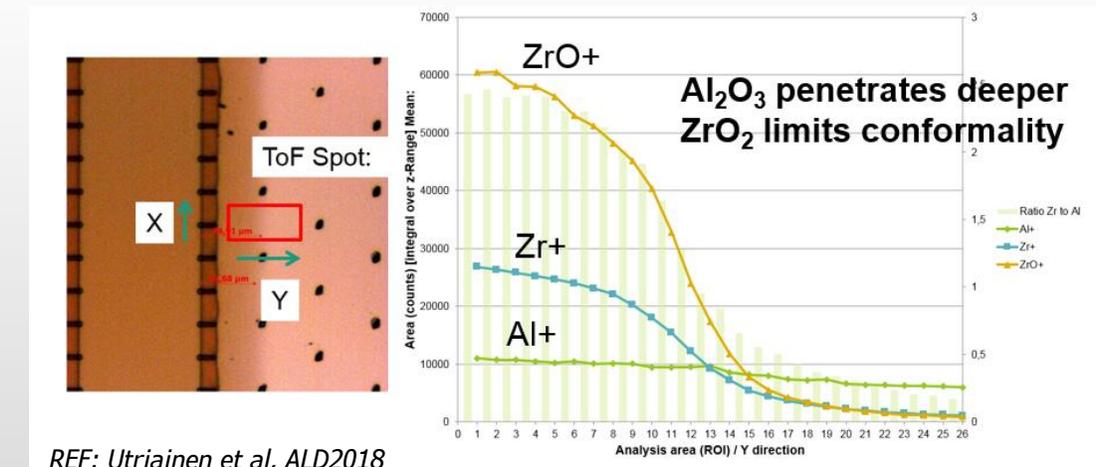
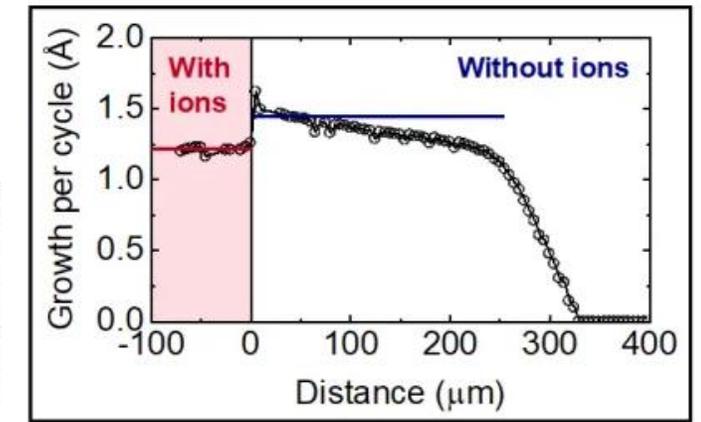
Scientific article references are listed in
www.pillarhall.com/references

Side view (during deposition)



Top view (membrane removed)

REF: Arts, K., in <https://www.atomiclimits.com/2020/11/11/understanding-plasma-ald-why-ions-matter-and-should-be-considered/>



REF: Utrainen et al, ALD2018

CONTACT

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NOTE: New OPEN DATA platform for ALD saturation profiles

<https://zenodo.org/communities/ald-saturation-profile-open-data/?page=1&size=20>

This is a place where you can share data with other scientists